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DESIGN OF PHASE-LOCKED LOOPS FOR DIGITAL SIGNAL PROCESSORS

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Abstract. *Digital signal processors (DSP) are widespread in real–time systems. In the last ten years phase–locked loops have widely been used in DSP as control devices correcting a clock skew. In this paper new type of floating phase locked loops for DSP is designed. For the floating phase locked loops new stability conditions are obtained.*
Keywords: Stability, Phase-locked loop, Processor, Clock skew

1. **Introduction.** Digital signal processors (DSP) are widespread in real–time systems [1]. In the last ten years phase–locked loops have widely been used in DSP as control devices correcting a clock skew. In this paper new type of floating phase locked loops for DSP are designed. Phase–locked loops (PLLs) are frequently encountered in radio engineering and communication. Once they had been invented in the 1930s–1940s [2–3], intensive studies of the theory and practice of PLLs were carried out [4–18].

In the last ten years, PLLs have been widely used in digital signal processors and other devices of digital information processing [19–26]. For example, there are such PLLs in the processors DSP 56000 and DSP 56 K (Motorola) [25, 26]. The PLLs showed their high efficiency as synthesizers of clock rates and as devices correcting a clock skew [19–26]. These properties of PLLs determine their specific features and their difference from the standard PLLs used in radio engineering. In this paper classical A. J. Viterbi ideas [4,7,8] for design of PLL with pulse modulation are developed and generalized. For this designed PLL necessary and sufficient conditions of global stability are obtained.

2. **Problem Statement and Preliminaries.** The main requirement to PLLs for digital signal processors is that they must be floating in phase. This means that the system must eliminate the clock skew completely.

Let us clarify the problem of eliminating a clock skew in multiprocessor systems when parallel algorithms are applied.

Consider a clock C that transmits clock pulses through a bus to processors P_k working in parallel (Fig. 1).

In realizing parallel algorithms, the processors must perform a certain sequence of operations simultaneously. These operations are to be started at the moment of arrival of clock pulses at a processor. Since the paths along which the pulses run from the clock to every processor are of different length, a noncoordination in time in the work of processors arises. This phenomenon is called a clock skew.