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REAL TIME DIGITAL CONTROLLER IMPLEMENTATION USING DETERMINISTIC UNIFORMLY WEIGHTED BIT STREAMS

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Abstract. *The problems associated with traditional real-time digital controllers can be overcome by the proposed controller implementation technique. The power of this technique essentially lies in the use of single-bit streams to represent the analogue signal instead of multi-bit words and requires elementary digital gates for controller implementation. The controllers can thus be implemented on Field Programmable Gate Arrays, FPGAs, or Application Specific integrated circuits, ASICs. The different elements of the bit-stream controller run in parallel and therefore guarantees real operation. Bit-stream controllers for a single-input-single-output, SISO, system have been presented. The design methodology is similar to continuous time controllers and also offers the versatility of digital systems. The inherently parallel nature of this technique also makes it possible to implement controllers for larger and more complex multiple-input-multiple-output, MIMO, systems.*

Keywords: Real-time systems, MIMO, Distributed systems, Digital control, Embedded systems

1. **Introduction.** Analogue building blocks comprising of amplifiers, integrators and the like can been constructed with operational amplifiers and passive components. There is a mature source of theory and tools [1] that facilitates the use of these kinds of elements in Single-Input-Single-Output, SISO, as well as Multiple-Input-Multiple-Output, MIMO, control systems. The availability of a variety of digital integrated circuits have made digital control systems [2] easier to implement.

Field Programmable Gate Array, FPGA or Application Specific Integrated Circuit, ASIC, technologies have made the implementation of artificial neural networks possible [3] [4] [5] but they still face routing and design fitting difficulties. These can be mitigated by bit-slicing [6] or bit-serialising [7] the data word e.g. an 8 bit word is sent to its destination over 8 clock cycles. The receiver must then accumulate these bits to reconstruct the full 8 bit word and process it normally. Alternatively, the 8 bit word could be sliced into 2 or 4 sections which the receiver can then reconstitute accordingly. In a multi-bit word environment, each processor is fairly complex requiring an appropriate arithmetic unit and may require some local RAM to store intermediate results. Bit-slicing necessarily introduces delays in the order of the number of slices which can be used advantageously by pipelined arithmetic units. However they are still reasonably complex. Bit-streams have been used in IIR filters [8]. This paper introduces some other ideas in