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A DESIGN OF NEURO-FUZZY INFERENCE CIRCUIT WITH AUTOMATIC GENERATION OF MEMBERSHIP FUNCTIONS

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Abstract. *In this paper, we propose a neuro-fuzzy inference circuit that generates membership functions and inference rules automatically in the learning process. In this circuit, we use membership functions which are generated by only using NOT operations and bit shift operations and tune only the parameters of the consequent part to reduce the circuit scale. In spite of those limitations, this circuit has high generalization ability obtained by generating new membership functions in the region with the maximum inference error. This circuit is designed by using hardware description language Verilog-HDL and realized on the FPGA(Field Programmable Gate array).*
Keywords: Neuro-fuzzy inference circuit, Field programmable gate array, Back-propagation algorithm, Self-tuning

1. **Introduction.** Recently, many researchers have studied fuzzy theory and its applications, because vague concepts and linguistic information can be dealt quantitatively in this theory [1-3]. So far, almost fuzzy inference systems have been implemented by computers software. The conventional software approach is large in size of system and the processing speed is low particularly in real-time systems. For this reason, the hardware implementation of fuzzy systems with high speed and high efficiency will be necessary for real-time use such as image and speech recognition [4-7]. So, we developed one of neuro-fuzzy inference circuits equipped with self-tuning of fuzzy inference rules [8]. We confirmed that the high speed inference and the high speed tuning of the inference rules are realized in this circuit. However, the generalization ability is deteriorated, because we used the fixed membership functions and tuned only the parameters of the consequent part to reduce the circuit scale.

In this paper, we propose a neuro-fuzzy inference circuit that generates the membership functions and the inference rules automatically in the learning process. In this circuit, we generate new membership functions in the region with the maximum inference error. Therefore, this circuit has a high generalization ability, even if the number of membership functions is small. In this circuit, we use the membership functions which are generated by only using NOT operations and bit shift operations to reduce the circuit scale. This circuit is designed by hardware description language Verilog-HDL and realized on the FPGA (Field Programmable Gate array).

2. **Previous Learning Algorithm [8].** In this section, we explain the learning algorithm which is used in fuzzy inference circuit proposed in [8].