

SMALL-WORLD NETWORK TO REDUCE DELAY IN FPGA ROUTING STRUCTURES

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ABSTRACT. *The performance of field-programmable gate arrays has improved dramatically owing to new process technologies. In new process technologies, interconnections dominate the delay in LSIs because of increased RC delay. To solve this problem, the development of an approach aiming to reduce wiring delay in deep submicron processes is very important and necessary. In this paper, we propose a novel routing structure using a small-world network for the interconnection of a field-programmable gate arrays. Using the small-world network leads to short distances between nodes and high connectivity among neighbors. The proposed routing structure has a few random wires that connect distant blocks and act as shortcuts. The results of an evaluation indicate that the proposed routing structure optimizes the critical path delay.*

Keywords: FPGA, Routing structure, Small-world network

1. Introduction. A field-programmable gate array (FPGA) is a programmable logic device (PLD) that can be used to implement any digital circuit after the manufacturing process. FPGAs are often used in electronic products such as audiovisual and communication equipments because they have lower nonrecurring engineering (NRE) costs and shorter time-to-market than application specific integrated circuits (ASICs). However, FPGAs have many problems, the most critical of which is wiring delay. The routing resources of FPGAs have essential redundancy to enable the implementation of as many types of circuits as possible. As a result, wiring delay accounts for the greatest part of the delay in FPGAs [1]. In addition, FPGAs are manufactured using new process technologies because large circuits require high-density for FPGA design. In deep submicron processes, the scaling down of the gate length and gate dielectric thickness reduce the gate delay small. In contrast, wiring delay increases due to increased resistance and capacitance. As a result, wiring delay dominates chip performance. This phenomenon is known as the interconnection crisis [2, 3].

At present, the interconnections of semiconductors are manufactured using low-resistivity material and low-k dielectric capacitance material in order to reduce the RC delay [4]. It is not sufficient to consider only PLDs (although this field of research is very important), and careful consideration must also be given to problems pertaining to the routing structure. In the conventional routing architecture of the FPGA, reducing the number of routing switches is important because switch delay is much larger than wiring delay. Wiring delay becomes more prominent in advanced processes. Consequently, a new architectural approach that focuses on reducing both wiring delay and the number of routing switches is effective and suitable for FPGAs involved in deep submicron processes. We have studied a novel routing structure for the interconnection of FPGAs by using the small-world network (SWN) order to reduce the wiring delay in deep submicron FPGAs