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A DIVIDING RATIO CHANGEABLE DIGITAL PLL WITH LOW JITTER USING PHASE STATE MEMORY

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Abstract. *In this paper, we propose a new dividing ratio changeable digital phase locked loop (DCPLL) with the low output jitter characteristic developed by considering the present phase state and the phase state before 1 period. The proposed DCPLL has an almost same circuit scale as the conventional DCPLL and the output jitter characteristic has always 1 pulse width of the base clock in a steady state. Our DCPLL can obtain an initial pull-in in one period of the input signal. Furthermore the multiplication output signal with the dispersive pulse interval can be obtained by using the remainder control circuit. We confirm the characteristics of our DCPLL by using a Field Programmable Gate Array (FPGA) based on Verilog-HDL descriptions.*
Keywords: Phase locked loop, All digital PLL, Field programmable gate array, Low jitter

1. **Introduction.** The phase locked loop (PLL) is used in various equipment, such as the extraction of timing waveforms in digital communication, the clock sources and the frequency synthesizers. In order to meet various kinds of demands regarding size, reliability and economy, PLL has been requested to be incorporated in system LSI over the past few years. Thus various kinds of all digital PLLs (ADPLL) were proposed [1-3].

In the ADPLL with the conventional basic structure, the dividing ratio is constant and the phase is controlled by adding or erasing base clock pulses. When many pulses are added or erased, the lock-in range can be expanded. However, since the resulting output jitter increases, the frequency of the output signal can not be varied widely from the center frequency. In addition, it takes a long time for lock-in and a circuit must be designed according to the frequency of the input signal. Various methods were proposed to solve this problem, but they can not solve the problem regarding the lock-in range [4,5].

Therefore, we proposed a dividing ratio changeable all digital PLL (DCPLL) with a wide lock-in range in our previous paper [6-8]. This circuit obtains the wide lock-in range compared to conventional PLL by changing the dividing ratio automatically according to the input frequency. But, the output jitter of this circuit is less than 3 pulses of the base clock in a steady state and the upper bound frequency of lock-in range is restricted by this output jitter in the conventional DCPLL.

In this paper, we propose a new DCPLL that obtains the low output jitter characteristic by memorizing the phase control state before 1 period of the input signal and by utilizing it in next period. Therefore, in the proposed DCPLL it is possible to improve the jitter