International Journal of Innovative Computing, Information and Control
Volume **5**, Number **11(A)**, November **2009**

ICIC International ©2009 ISSN 1349-4198
pp. **3961–3969**

AN EFFECTIVE IMMUNE ALGORITHM FOR MULTIPLE-VALUED LOGIC MINIMIZATION PROBLEMS

Shangce Gao[1], Zheng Tang[1] and Catherine Vairappan[2]

[1]Graduate School of Innovation Life Science
University of Toyama
Gofuku 930-8555, Toyama-shi, Japan
d0881103@ems.u-toyama.ac.jp; ztang@eng.u-toyama.ac.jp

[2]Tateyama Institute of System
Yanagi 930-0016, Toyama-shi, Japan
ckuramitz@hotmail.com

Received July 2008; revised November 2008

Abstract. *This paper presents an algorithm based on an artificial immune system to minimize the multiple-valued logic (MVL) functions. In the proposed algorithm, the length of antibody (solution) is adaptive in order to reduce the computational complexity. The affinity function is designed to consist of two metrics (correctness and optimality) so that the average number of product terms in the solution can be efficiently minimized. Furthermore, both the proportional clone operator and random hypermutation carry out the affinity maturation. Simulation results based on a great amount of MVL functions demonstrate the efficiency of the proposed method.*
Keywords: Multiple-valued logic, Immune algorithm, Logic minimization

1. **Introduction.** Multiple-valued logic (MVL) has been the subject of much research over many years. It is a way of implementing digital operations by using a multiple set of logical values {0,1,2,3,...} instead of the binary set {0,1}. The performance of two levels (binary logic) is limited due to interconnections, which occupy a large area on a VLSI chip. In a VLSI chip, approximately seventy percent of the area is devoted to interconnection, twenty percent to insulation and ten percent to device [1], [2]. One can achieve a more cost-effective way of utilizing interconnections by using a larger set of signals over the same area in MVL. This also solves the problem of pin-out (the limit to the amount of data that can enter and exit a chip). Besides reductions in interconnection and chip area, multiple-valued logic networks have emerged as powerful image processing [3] and speech recognition techniques [4].

The logic process of MVL is much more complicated than that of binary logic, so the MVL is expected to be more powerful for implementing digital functions with a smaller number of devices. The main drawback of MVL devices is that their design techniques are more complicated than those of binary logic devices [5]. The minimization of MVL functions is an important technique for reducing the area required by a programmable logic array [6]. The decision for this task is possible due to the minimization of logic function and thus the algorithms depend on the functional completeness basis in which the circuit for the given function will be realized.

In the literature, there are several methodologies reported for synthesis of MVL functions, such as deterministic algorithms [7], direct cover based approaches [8], [9], [23], network learning using local search method (LS) [10], [11], genetic algorithms [12], [13],