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QUANTUM-INSPIRED EVOLUTIONARY DESIGN OF SYNCHRONOUS FINITE STATE MACHINES: PART II

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Abstract. *Synchronous finite state machines are very important for digital sequential designs. Among other important aspects, they represent a powerful way for synchronizing hardware components so that these components may cooperate adequately in the fulfillment of the main objective of the hardware design. In this paper, we propose an evolutionary methodology based on the principles of quantum computing to synthesize finite state machines. First, we optimally solve the state assignment NP-complete problem, which is inherent to designing any synchronous finite state machines. This is motivated by the fact that with an optimal state assignment, one can physically implement the state machine in question using a minimal hardware area and response time. Second, with the optimal state assignment provided, we propose to use the same evolutionary methodology to yield an optimal evolutionary hardware that implements the state machine control component. The evolved hardware requires a minimal hardware area and imposes a minimal propagation delay on the machine output signals. This work is divided in a two-part paper: the assignment problem was approached in Part I* [1] *while the generation of the control logic is fully deployed in this part of the paper.*

Keywords: Finite state machine, Quantum computing, Evolutionary algorithms, Control synthesis

1. Introduction.

This paper is continuation of Part I [1], in which we concentrated our effort on the third step or state assignment, of the state machine design methodology. In this part of the paper, we dedicate ourselves to the fourth step of the design process, that is the automatic generation of the control logic circuit minimization problems. We apply the quantum-inspired genetic algorithm, described in details in [1], to solve this problem and show the obtained promising results.

The control logic component in a state machine is responsible for generating the primary output signals as well as the signal that form the next state. It does so using the primary input signals and the signals that constitute the current state. Traditionally, the combinational circuit of the control logic is obtained using the transition maps of the flip-flops [2, 3]. Given a state transition function, it is expected that the complexity, in terms of area and time, and so the cost of the control logic will vary for different assignments of flip-flop combinations to the allowed states. Consequently, the designer should seek the assignment that minimizes the complexity and so the cost of the combinational logic required to control the state transitions.

The designer or the computer-aided design tool for circuit synthesis needs always to select carefully the state assignment to be used. Existing techniques for state assignment can be listed as follows: *one-hot* [4], the use of *heuristics* [5, 6] and *meta-heuristics* [7, 8].