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EFFECTS OF GATE TUNNELING CURRENT ON THE STATIC CHARACTERISTICS OF CMOS CIRCUITS

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Abstract. *With the scaling of MOS devices, gate tunneling current increases in exponential with thinner gate oxides, and the static standby power consumption of CMOS circuits is severely affected by the presence of gate tunneling currents. To illustrate the impacts, in this paper, a simpler gate tunneling current theory model by a double integral approach in ultra-thin gate oxide MOS devices that tunneling current changes with gate-oxide thickness is presented. The simulation results well agree with the theory model proposed in BSIM4. The characteristics of current source inverter composed of ultra-thin gate oxide MOS devices are also studied in detail to analyze its behavior and predict the trends of power dissipated with scaled technology nodes in the effects of gate tunneling current.*

Keywords: Device simulation, Gate tunneling current model, Static power consumption, Ultra-thin gate oxide

1. **Introduction.** The size of MOS transistors has reached the point where gate tunneling currents become important due to the reduced gate dielectric thickness [1]. Aggressive scaling of MOS devices requires use of ultra-thin gate oxides to maintain a reasonable short channel effect [2]. The International Technology Roadmap for Semiconductors (ITRS) predicts gate-oxide thicknesses less than 1.4nm for sub-100-nm CMOS which results in considerable direct tunneling current [3,4]. For CMOS devices with thinner oxides, the gate-to-channel tunneling current becomes appreciable and dominates the total static state leakage of the transistor [5]. It is clear from the literatures that gate tunneling has been extensively modeled but some studies focused mainly on the theory of tunneling and the equations developed were not suitable for predicting behavior and trends by simulation due to their complexity [6-9]. Also, assumptions such as ignoring tunneling in the PMOSFET and tunneling in the gate overlap regions were made [10-12].

In this paper, following a double integral approach, a simpler gate tunneling current model that reveals the relations between gate tunneling current and oxide thickness is proposed, and the impact of gate tunneling current on a current source inverter is studied in detail. Considering the tunneling currents of the NMOSFET and PMOSFET in the gate and the gate-overlap regions, the degradation characteristics of MOS devices is simulated, and the effect of gate tunneling current in ultra-thin gate oxide MOS devices of dielectric thickness of 0.7, 0.8, 0.9, 1.1, 1.2 and 1.3nm corresponding to 40, 45, 53, 65, 75 and 90nm gate length is studied using device simulation, respectively. The degradation of inverter in performance is measured in terms of output voltage swing and power consumption