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ADAPTIVE FRAME LENGTH METHOD FOR HARDWARE CONTEXT-SWITCHING IN DYNAMIC PARTIAL SELF-RECONFIGURABLE SYSTEMS

Trong-Yen Lee[1], Che-Cheng Hu[1], Yang-Kun Huang[1] and Chia-Chun Tsai[2]

[1]Graduate Institute of Computer and Communication
National Taipei University of Technology
No. 3, Zhongxiao E. Road, Taipei 10643, Taiwan
{ tylee; s4419010; t5418065 }@ntut.edu.tw

[2]Department of Computer Science and Information Engineering
Nanhua University
No. 55, Sec. 1, Nanhua Road, Zhongkeng, Dalin Township, Chia-Yi 62248, Taiwan
chun@mail.nhu.edu.tw

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Abstract. *A dynamically and partially reconfigurable system can arbitrarily swap hardware tasks at runtime. However, such FPGA systems require a long time to read and much memory to store the hardware context, when a hardware task is swapped out. A solution to this problem is to adjust the amount of read-back data in a hardware task to reduce the required memory size and reconfiguration time. Therefore, this investigation develops an adaptive frame length method for hardware context-switching with a context reading and writing (CRW) algorithm in dynamically partial self-reconfigurable (DPSR) FPGA systems. The proposed CRW algorithm requires less instruction to execute Readback and Writeback procedures. Therefore, the CRW algorithm is one means of reducing reconfiguration time. Experimental results show that the proposed method reduces hardware reconfiguration time by 7.763%, memory size by 63.79% and resource overhead by 47.33%.*

Keywords: Context-switching, Dynamic partial self-reconfigurable system, Readback, Reconfiguration time, Memory size

1. **Introduction.** *Field programmable gate arrays* (FPGAs) that execute at least two hardware tasks simultaneously are very popular in the design of embedded systems. *Dynamically partial self-reconfigurable* (DPSR) FPGAs allow for the reconfiguring of various hardware tasks at runtime using early access partial reconfiguration [1] whenever DPSR FPGA systems have placement and removal requirements. Therefore, the release of hardware space at runtime is critical. DPSR FPGA systems can thus perform partial reconfiguration and share FPGA resources among hardware tasks. These useful features can be applied to save and restore register information in DPSR FPGA systems, which process is called hardware context-switching.

Hardware context-switching enables hardware resources to be replaced when new high-priority tasks are to be executed. Hardware tasks can also be reloaded to complete unfinished work whenever a request is made for swap-in by context-switching. Additionally, a hardware task consists of many configurable logics. For this reason, swap-out by context-switching requires huge memory to save all of the registers of the configurable logics that are associated with the hardware task. Therefore, the two main disadvantages of the DPSR FPGA system are the time delay that is associated with the hardware