International Journal of Innovative
Computing, Information and Control
Volume **7**, Number **9**, September **2011**

ICIC International ©2011 ISSN 1349-4198
pp. 5145–5161

HIGH PERFORMANCE BUFFERED X-ARCHITECTURE ZERO-SKEW CLOCK TREE CONSTRUCTION WITH VIA DELAY CONSIDERATION

Chia-Chun Tsai[1], Chung-Chieh Kuo[2] and Trong-Yen Lee[2]

[1]Department of Computer Science and Information Engineering
Nanhua University
No. 55, Sec. 1, Nanhua Rd., Zhongkeng, Dalin Township, Chia-Yi 62248, Taiwan
chun@mail.nhu.edu.tw

[2]Graduate Institute of Computer and Communication
National Taipei University of Technology
No. 1, Sec. 3, Chung-hsiao E. Rd., Taipei 10608, Taiwan
{ s4419014; tylee }@ntut.edu.tw

Received April 2010; revised August 2010

Abstract. *As VLSI technology advances into nanometer dimensions, clock routing becomes a limiting factor in determining chip performance. To deal with the challenge, X-architecture has been proposed and widely applied in routing field because it contributes more improvements in terms of the clock delay, wirelength, and power consumption than general Manhattan-architecture. This work proposes an X-architecture zero-skew clock tree construction with buffer insertion/sizing and wire sizing, called a BIS-X algorithm. Differing from other buffer-insertion works, the delay of vias is considered in clock delay calculation. Given a set of n clock sinks with an X-pattern library and a B-type buffer library, an X-pattern matching technique is first used for connecting the paired sinks. Next, two unit-size buffers are respectively inserted into the left and right branches of a tapping point. Then, the inserted buffers are sized for branch delay improvement. Furthermore, X-Flip and wire sizing techniques are sequentially applied for reducing wirelength and keeping zero skew. The proposed BIS-X algorithm can construct a buffered X-architecture zero-skew clock tree level-by-level with minimum delay in* $O(B^2 n \log n)$. *As reported in the experimental results on benchmarks, our BIS-X averagely reduces clock delay by 32.6%-69.4%, compared with other buffered clock routing algorithms.*
Keywords: Buffer insertion, Clock routing, X-architecture

1. **Introduction.** As VLSI technology enters deep submicron (DSM) era, interconnect delay plays an important role in chip performance. A clock signal is employed in a VLSI system for synchronizing the actions of the intrinsic designs or intellectual properties (IPs). Therefore, designers should minimize clock delay and make zero skew to prevent fault functions induced by the different arrival times. In real-time VLSI systems, phase-locked loops (PLLs) have been widely used in digital signal processors (DSPs) as control devices correcting a clock skew [1,2]. Tsay [3] constructed a zero-skew tree (ZST) for a given set of clock sinks based on Manhattan-architecture. His method recursively connects two sub-ZSTs with a determined tapping point to construct a larger ZST. The process of tapping-point determination relates to a zero-skew ratio x. When $0 \leq x \leq 1$, the tapping point locates on the wire that connects two sub-ZSTs. When $x < 0$ or $x > 1$, the tapping point right locates at one of two sub-ZSTs and a snaking wire is required for clock skew compensation. The deferred merge embedding (DME) algorithm [4] follows Tsay's method [3] to minimize the total wirelength whereas zero skew is also maintained.