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A STEP-DOWN SWITCHED-CAPACITOR AC-DC CONVERTER WITH DOUBLE CONVERSION TOPOLOGY

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Abstract. *In the field of portable electronic devices, a small and light AC-DC converter or AC adapter has been required in these last few decades. To meet such demands, a switched-capacitor (SC) AC-DC converter draws many researchers' attentions in recent years. It is known that the SC AC-DC converter can realize smaller size and lighter weight than transformer-based AC-DC converters, because no magnetic component is required to design the SC AC-DC converter. In previous studies, several AC-DC converters succeeded in downsizing and light-weighting by using SC techniques. However, the power efficiency of conventional SC AC-DC converters is still low, and their control method is complicated. To overcome these problems, a step-down SC AC-DC converter with double conversion topology is proposed in this paper. The proposed converter consists of a full waveform rectifier with a big capacitor and two converter blocks. In each converter block, the* $1/3\times$ *step-down conversion is performed by connecting three capacitors in series, where electric charges stored in these capacitors are averaged by using series-connected flying capacitor. By connecting these converter blocks in series, the* $1/9\times$ *step-down conversion is realized by controlling power switches by non-overlapped two-phase clock pulses. Therefore, unlike the conventional converters using multiphase clock pulses, the proposed converter can achieve not only simple circuit control but also small ripple noise. Furthermore, the reduction of output ripple leads to the improvement of power efficiency. To help readers' understanding for the proposed converter, first, a simple four equivalent circuit of the proposed converter is derived theoretically. The characteristics of the proposed converter are clarified by the theoretical analysis. Then, in order to demonstrate the effectiveness of the proposed converter, the proposed converter is implemented by simulated program with integrated circuit emphasis (SPICE) simulator. The validity of the theoretical results is confirmed by the SPICE simulation. Finally, the feasibility of the proposed converter is confirmed by experiments implemented on a breadboard.*
Keywords: AC-DC converters, Switched capacitor circuits, Inductor-less circuits, Series-connected converters, Flying capacitors

1. **Introduction.** In recent years, a low voltage such as DC 12V is used to drive portable applications. However, an AC voltage supplied by a commercial power source is much

higher than 12V. For example, the commercial power source is 100V@50/60Hz in Japan. To provide the DC 12V by converting the AC voltage, an AC adapter, AC-DC adapter, or AC-DC converter is usually used as an external power supply. Hence, the AC-DC converter is indispensable for the small power application such as mobile devices. In past studies, various types of AC-DC converters have been proposed. For example, Yang and Lin proposed a high step-down AC-DC converter [1]. The high step-down AC-DC converter can offer a high power factor and high step-down conversion ratio by modifying the boost and the buck-boost converters [2-6]. However, in the field of mobile applications, the demand for small and lightweight AC-DC converter is increasing rapidly in recent years. Unfortunately, traditional AC-DC converters, which have magnetic components, cannot satisfy such demands, because the magnetic component is heavy and bulky. To solve this problem, an AC-DC converter designed by switched-capacitor (SC) techniques has been developed [7-12], because the magnetic component is not required in the design of the SC power converter.

To the best of our knowledge, Ueno et al. proposed the first SC AC-DC converter in 1989 [13]. The AC-DC converter generates the n times stepped-up voltage, where n $(= 2, 3, \ldots)$ is the number of capacitors composing the AC-DC converter. On the basis of this study, Oota et al. suggested the step-down SC AC-DC converter [14, 15]. Although the circuit topology of the step-down SC AC-DC converter is the same as that of the first SC AC-DC converter, the control method is improved to generate a stepped-down voltage. The operation principle of the step-down SC AC-DC converter is as follows: 1) all capacitors are connected in series so that an input voltage will be divided by each series-connected capacitor; 2) all capacitors are connected with an output load in parallel so that each capacitor will provide a stepped-down voltage to the output load. By repeating these steps, the step-down SC AC-DC converter [14, 15] generates a stepped-down voltage. Therefore, the output voltage of the step-down SC AC-DC converter becomes one n-th of the input voltage, where n is the number of capacitors. However, all capacitors must have a large capacitance so that the SC AC-DC converter [14, 15] can achieve high voltage efficiency. Furthermore, since the step-down ratio of the SC AC-DC converter [14, 15] depends on the number of capacitors, many circuit components are required to realize a large step-down ratio. To overcome these problems, Eguchi et al. developed a series-parallel type SC AC-DC converter [16]. Owing to the series-parallel topology, the series-parallel type converter [16] can reduce the number of capacitors. However, the series-parallel type SC AC-DC converter [16] still requires many circuit components. To reduce the number of circuit components, we proposed a step-down SC AC-DC converter with series-connected converter blocks [17]. Owing to series-connected topology, the SC AC-DC converter [17] can achieve the smallest number of circuit components among the previous SC AC-DC converters [14-17]. By converting the AC input twice, the SC AC-DC converter reported in [17] offers the $1/9$ $(= (1/3)^2)\times$ stepped-down voltage with the small number of circuit components. However, the series-connected converter [17] suffers from complex switching control and large ripple noise, because the power switches are controlled by multiphase clock pulses. Furthermore, its power efficiency is low due to large ripple noise.

In this paper, a novel step-down SC AC-DC converter is proposed to solve the problems of conventional SC AC-DC converters. The proposed converter consists of a full waveform rectifier with a big capacitor and two converter blocks. In each converter block, the $1/3\times$ step-down conversion is performed by connecting three capacitors in series, where electric charges stored in these capacitors are averaged by utilizing series-connected flying capacitor. By connecting these converter blocks in series, the $1/9\times$ step-down conversion is realized by controlling power switches by non-overlapped two-phase clock pulses. Owing

to the new circuit topology, the proposed converter can achieve not only smaller ripple noise but also higher power efficiency than the conventional converter. These advantages are confirmed by circuit simulations using the simulated program with integrated circuit emphasis (SPICE) simulator. Then, in order to help readers' understanding, a simple four equivalent model of the proposed converter is derived theoretically. Furthermore, to confirm the feasibility of the proposed converter, experiments are demonstrated concerning the proposed converter built on a breadboard.

This paper consists of six sections. In Section 2, both the conventional converter and the proposed converter are detailed to clarify the difference of circuit topology between them. The equivalent model of the proposed converter is obtained theoretically in Section 3. Sections 4 and 5 describe the SPICE simulated results and experimental results. Finally, the results of this study are summarized in Section 6.

2. Circuit Configuration.

2.1. Conventional SC AC-DC converter. Figure 1 illustrates the circuit configuration of the conventional SC AC-DC converter reported in [17]. As Figure 1 shows, the conventional converter consists of a full bridge circuit and two converter blocks, where 12 power switches, 9 capacitors, and 4 diodes are required. The output voltage of the conventional converter is expressed as

$$V_o = V_{o2} = \frac{1}{9}V_i,$$
$$\text{where } V_{o2} = \frac{1}{3}V_{i2},\ V_{i2} = V_{o1} \text{ and } V_{o1} = \frac{1}{3}V_{i1}. \tag{1}$$

In (1), V_{i1} is the output voltage of the full bridge circuit, V_{o1} $(= V_{i2})$ is the output voltage of the converter block-1, and V_o $(= V_{o2})$ is the output voltage of the converter block-2. As (1) shows, the conventional converter reported in [17] can realize higher step-down gain than the previous converters proposed in [13-16] by converting V_{i1} twice. In each converter block, each input voltage is divided by the main capacitors $C_{i,2}$, $C_{i,3}$ and $C_{i,4}$ $(i = 1, 2)$. By connecting the flying capacitor $C_{i,1}$ in turn to the main capacitors, the electric charges stored in the main capacitors are averaged, where the conventional converter has three states in one cycle of the operation. Therefore, the $1/3\times$ step-down conversion is realized by each converter block. By connecting these converter blocks in series, the output voltage V_o becomes $1/9$ $(= (1/3)^2)$ of the input voltage. However, the

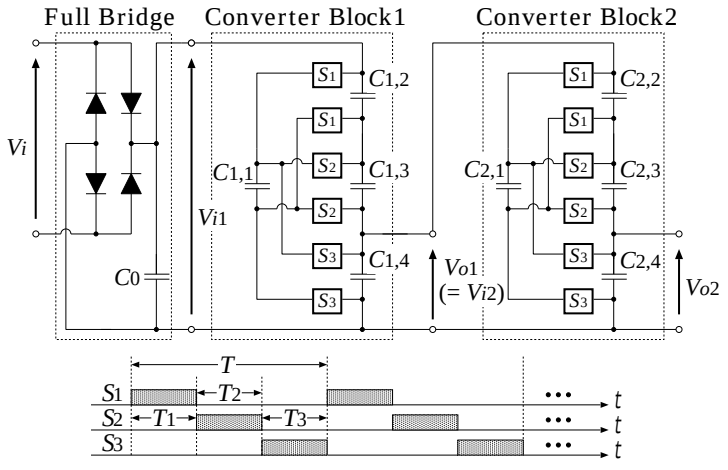


FIGURE 1. Conventional SC AC-DC converter proposed in [17]

electric charge is offered to the capacitor $C_{i,4}$ at only one of three states (see in Figure 1). For this reason, the conventional converter suffers from complex switching control and large ripple noise. Furthermore, it is difficult to achieve high power efficiency due to the large ripple noise.

2.2. **Proposed SC AC-DC converter.** Figure 2 illustrates the circuit configuration of the proposed SC AC-DC converter, where the output voltage of the proposed converter is the same as (1). As Figure 2 shows, the proposed converter consists of 12 power switches, 11 capacitors, and 4 diodes. In the proposed converter, the $1/9\times$ step-down conversion is realized by utilizing series-connected flying capacitors $C_{i,1}$ and $C_{i,2}$ $(i = 1, 2)$. In each converter block, the main capacitors $C_{i,3}$, $C_{i,4}$ and $C_{i,5}$ work as a capacitive voltage divider, where electric charges stored in these capacitors are averaged by using non-overlapped two-phase clock pulses. Concretely, in State-T_1, the flying capacitors $C_{i,1}$ and $C_{i,2}$ are connected to the main capacitors $C_{i,3}$ and $C_{i,4}$ in parallel. On the other hand, in State-T_2, $C_{i,1}$ and $C_{i,2}$ are connected to the main capacitors $C_{i,4}$ and $C_{i,5}$ in parallel. Therefore, unlike the conventional converter, the electric charge is offered to the capacitor $C_{i,5}$ at one of two states (see in Figure 2). For this reason, the proposed converter can achieve not only smaller ripple noise but also higher power efficiency than the conventional converter. Furthermore, the proposed converter can offer the simple circuit control using two-phase clock pulses.

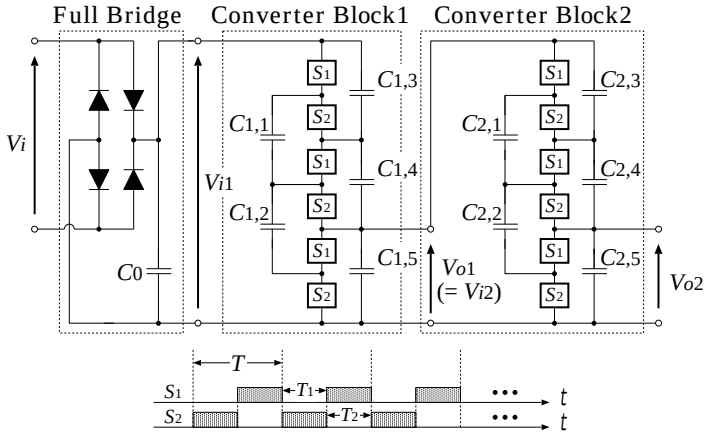


FIGURE 2. Proposed SC AC-DC converter

3. **Theoretical Analysis.** To help readers' understanding for the proposed converter, a simple four equivalent circuit of the proposed converter is derived theoretically. In the theoretical analysis, the equivalent circuit is assumed as a four-terminal equivalent model reported in [18-20], where we make the following assumptions to simplify the theoretical analysis: 1) an ac input is a staircase ac waveform; 2) all of circuit components have negligibly small parasitic elements; and 3) the circuit has time constant so larger than a period of clock pulses. The four-terminal equivalent model is shown in Figure 3. In Figure 3, V_{in} is the input voltage, V_{out} is the output voltage, m_1 is the turn ratio of an ideal transformer, R_{SC} is the internal resistance of the power converter, and R_L is the output load. In the theoretical analysis, the parameters m_1 and R_{SC} are obtained as follows.

Figure 4 illustrates the instantaneous equivalent circuits of the series-connected converter blocks. As Figure 4 shows, the proposed converter has two states in T_i $(i = 1, 2)$. In a steady state, the electric charge in $C_{1,k}$ and $C_{2,k}$ $(k = 1, \ldots, 5)$ has to be the same at

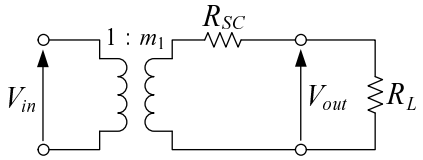


FIGURE 3. Four-terminal equivalent model

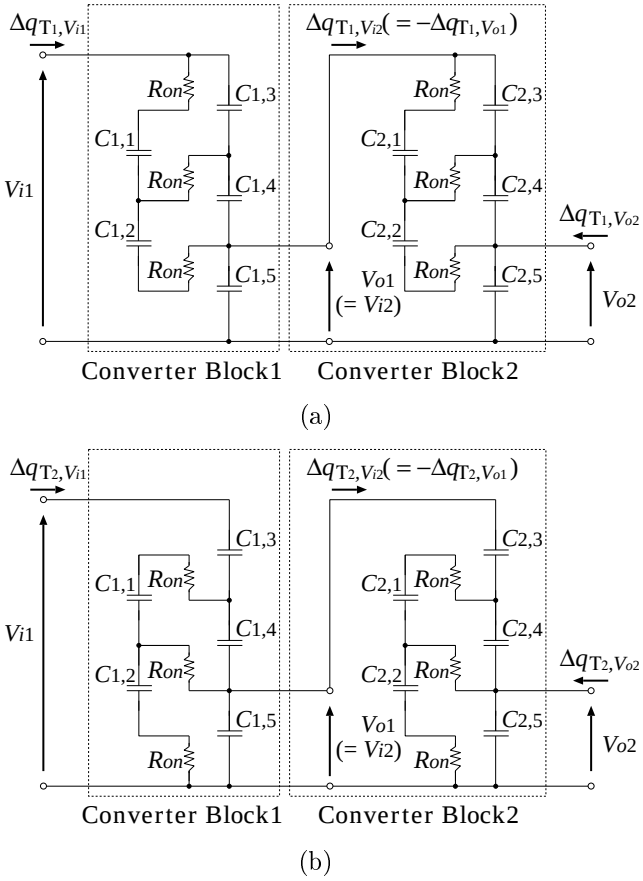


FIGURE 4. Instantaneous equivalent circuits of the converter blocks: (a) State-T_1 and (b) State-T_2

the start and end of the cycle T. Therefore, the differential value of the electric charge in $C_{1,k}$ satisfies the following conditions:

$$\sum_{i=1}^{2} \Delta q_{T_i}^{1,k} = 0 \text{ and } \sum_{i=1}^{2} \Delta q_{T_i}^{2,k} = 0,$$
$$\text{where } T = \sum_{i=1}^{2} T_i \text{ and } T_1 = T_2 = \frac{T}{2}. \tag{2}$$

In (2), $\Delta q_{T_i}^{1,k}$ and $\Delta q_{T_i}^{2,k}$ denote the electric charge of the k-th capacitor in State-T_i. In the converter block-1, the differential values of electric charges in V_{i1} and V_{o1}, $\Delta q_{T_i,V_{i1}}$ and $\Delta q_{T_i,V_{o1}}$, are given by

$$\Delta q_{T_1,V_{i1}} = \Delta q_{T_1}^{1,1} + \Delta q_{T_1}^{1,3} = \Delta q_{T_1}^{1,2} + \Delta q_{T_1}^{1,4},$$

$$\begin{aligned}
\Delta q_{T_1,V_{o1}} &= \Delta q_{T_1}^{1,5} - \Delta q_{T_1}^{1,2} - \Delta q_{T_1}^{1,4}, \\
\Delta q_{T_2,V_{i1}} &= \Delta q_{T_2}^{1,3} = \Delta q_{T_2}^{1,1} + \Delta q_{T_2}^{1,4}, \\
\text{and} \quad \Delta q_{T_2,V_{o1}} &= \Delta q_{T_2}^{1,5} - \Delta q_{T_2}^{1,1} + \Delta q_{T_2}^{1,2} - \Delta q_{T_2}^{1,4}.
\end{aligned} \tag{3}$$

On the other hand, in the converter block-2, the differential values of electric charges in V_{i2} and V_{o2}, $\Delta q_{T_i,V_{i2}}$ and $\Delta q_{T_i,V_{o2}}$, are given by

$$\begin{aligned}
\Delta q_{T_1,V_{i2}} &= \Delta q_{T_1}^{2,1} + \Delta q_{T_1}^{2,3} = \Delta q_{T_1}^{2,2} + \Delta q_{T_1}^{2,4}, \\
\Delta q_{T_1,V_{o2}} &= \Delta q_{T_1}^{2,5} - \Delta q_{T_1}^{2,2} - \Delta q_{T_1}^{2,4}, \\
\Delta q_{T_2,V_{i2}} &= \Delta q_{T_2}^{2,3} = \Delta q_{T_2}^{2,1} + \Delta q_{T_2}^{2,4}, \\
\text{and} \quad \Delta q_{T_2,V_{o2}} &= \Delta q_{T_2}^{2,5} - \Delta q_{T_2}^{2,1} + \Delta q_{T_2}^{2,2} - \Delta q_{T_2}^{2,4}.
\end{aligned} \tag{4}$$

Using (2)-(4), the average input currents and the average output currents can be expressed as

$$\begin{aligned}
&\overline{I_{i1}} = \frac{1}{T}\left(\sum_{i=1}^{2} \Delta q_{T_i,V_{i1}}\right) = \frac{\Delta q_{V_{i1}}}{T}, \qquad \overline{I_{i2}} = \frac{1}{T}\left(\sum_{i=1}^{2} \Delta q_{T_i,V_{i2}}\right) = \frac{\Delta q_{V_{i2}}}{T}, \\
&\overline{I_{o1}} = \frac{1}{T}\left(\sum_{i=1}^{2} \Delta q_{T_i,V_{o1}}\right) = \frac{\Delta q_{V_{o1}}}{T}, \quad \text{and} \quad \overline{I_{o2}} = \frac{1}{T}\left(\sum_{i=1}^{2} \Delta q_{T_i,V_{o2}}\right) = \frac{\Delta q_{V_{o2}}}{T},
\end{aligned} \tag{5}$$

where $\Delta q_{V_{i1}}$, $\Delta q_{V_{i2}}$, $\Delta q_{V_{o1}}$ and $\Delta q_{V_{o2}}$ are electric charges in the input/output terminals. Substituting (2)-(4) into (5), we have the relation between the input current and output current as follows:

$$\begin{aligned}
&\overline{I_{i1}} = -\frac{1}{9}\overline{I_{o2}}, \\
&\text{where} \quad \Delta q_{V_{o1}} = -\Delta q_{V_{i2}}, \ \Delta q_{V_{i1}} = -\frac{1}{3}\Delta q_{V_{o1}}, \ \text{and} \ \Delta q_{V_{i2}} = -\frac{1}{3}\Delta q_{V_{o2}}.
\end{aligned} \tag{6}$$

From (6), the parameter m_1 of Figure 3 is obtained as

$$m_1 = \frac{1}{9}, \tag{7}$$

because the parameter m_1 denotes the turn ratio of an ideal transformer.

Next, the parameter R_{SC} is derived by considering the consumed energy of the converter blocks in one period. From Figure 4(a), the consumed energy in State-T_1, W_{T_1}, can be obtained by

$$\begin{aligned}
W_{T_1} &= \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^{1,1}\right)^2 + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^{1,1} - \Delta q_{T_1}^{1,2}\right)^2 + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^{1,2}\right)^2 \\
&\quad \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^{2,1}\right)^2 + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^{2,1} - \Delta q_{T_1}^{2,2}\right)^2 + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^{2,2}\right)^2 \\
&= \frac{40R_{on}}{54T_1}(\Delta q_{V_{o2}})^2.
\end{aligned} \tag{8}$$

On the other hand, from Figure 4(b), the consumed energy in State-T_2, W_{T_2}, can be obtained by

$$\begin{aligned}
W_{T_2} &= \frac{R_{on}}{T_2}\left(\Delta q_{T_2}^{1,1}\right)^2 + \frac{R_{on}}{T_2}\left(\Delta q_{T_2}^{1,1} - \Delta q_{T_2}^{1,2}\right)^2 + \frac{R_{on}}{T_2}\left(\Delta q_{T_2}^{1,2}\right)^2 \\
&\quad \frac{R_{on}}{T_2}\left(\Delta q_{T_2}^{2,1}\right)^2 + \frac{R_{on}}{T_2}\left(\Delta q_{T_2}^{2,1} - \Delta q_{T_2}^{2,2}\right)^2 + \frac{R_{on}}{T_2}\left(\Delta q_{T_2}^{2,2}\right)^2
\end{aligned}$$

$$= \frac{40R_{on}}{54T_2}(\Delta q_{V_{o2}})^2. \tag{9}$$

By combining (8) and (9), we have the total consumed energy as follows:

$$W_T = \sum_{i=1}^{2} W_{T_i} = \frac{80R_{on}}{27T}(\Delta q_{V_{o2}})^2. \tag{10}$$

In Figure 3, the consumed energy of the four-terminal equivalent model is defined by

$$W_T := \left(\frac{\Delta q_{V_o}}{T}\right)^2 \cdot R_{SC} \cdot T, \tag{11}$$

because the ideal transformer is a lossless component. By comparing (10) with (11), the parameter R_{SC} of the series-connected converter blocks is obtained as follows:

$$R_{SC} = \frac{80R_{on}}{27}. \tag{12}$$

Using (7) and (12), we have the four-terminal equivalent model. The equivalent model of the series-connected converter blocks can be expressed by the following K-matrix:

$$\begin{bmatrix} \overline{V_i} \\ \overline{I_i} \end{bmatrix} = \begin{bmatrix} 9 & 0 \\ 0 & 1/9 \end{bmatrix} \begin{bmatrix} 1 & 80R_{on}/27 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{o2}} \\ -\overline{I_{o2}} \end{bmatrix}. \tag{13}$$

From (13), we can estimate the maximum power efficiency η and the maximum output voltage V_{out} as follows:

$$\eta = \frac{R_L}{R_L + 80R_{on}/27} \text{ and } V_{out} = \left(\frac{R_L}{R_L + 80R_{on}/27}\right) \times \frac{V_{in}}{9}. \tag{14}$$

As you can see from (14), the power efficiency depends on the internal resistance R_{SC}. In other words, R_{SC} is one of the most important factors to realize high power efficiency.

Table 1 shows the comparison of the internal resistances between the proposed converter and the conventional converters reported in [14] and [17]. As Table 1 shows, the internal resistance of the proposed converter is smaller than that of the conventional converters. Therefore, the proposed converter can achieve the highest power efficiency among them. On the other hand, the power efficiency of the conventional converter reported in [17] is the worst. However, the number of circuit components for the conventional converter [17] is the smallest. Table 2 shows the comparison of the number of circuit components between the proposed converter and the conventional converters [14, 17]. As you can see

TABLE 1. Comparison of the internal resistances

	R_{SC}	Step-down ratio
Proposed converter	$80R_{on}/27$	1/9
Conventional converter [14]	$280R_{on}/81$	1/9
Conventional converter [17]	$40R_{on}/9$	1/9

TABLE 2. Comparison of the number of circuit components

	Power switch	Capacitor	Diode	Total
Proposed converter	12	11	4	27
Conventional converter [14]	28	10	4	42
Conventional converter [17]	12	9	4	25

from Table 2, the proposed converter requires two capacitors more from the conventional converter reported in [17], because the proposed converter has four flying capacitors.

4. **Simulation.** To investigate the characteristics of the proposed converter, circuit simulations using the SPICE simulator are performed concerning output voltages and power efficiency. Furthermore, by comparing the characteristics of the proposed converter with that of the conventional converters [14] and [17], the effectiveness of the proposed topology is confirmed. In the SPICE simulations, the following conditions were used: $V_{in} = 100\text{V@50Hz}$, $T = 1\mu\text{s}$, $R_{on} = 0.1\Omega$, $C_0 = 99\mu\text{F}$ and $C_{1,k} = C_{2,k} = 33\mu\text{F}$.

Figure 5 demonstrates the simulated output voltage of the proposed converter as a function of time. In Figure 5, a stepped-down DC voltage is provided to the output load R_L $(= 10\Omega)$. The comparison of output voltages between the proposed converter and the conventional converters [14] and [17] is shown in Figure 6. As Figure 6 shows, the output voltage of the proposed converter is the highest among them. In other words, the proposed converter can achieve higher voltage efficiency than the conventional converters. Of course, as Table 1 shows, the output voltage depends on the internal resistance R_{SC}.

Figure 7 shows the comparison of output ripples between the proposed converter and the conventional converters [14] and [17]. Obviously, the output ripple of the proposed converter is smaller than that of the conventional converters. Owing to the simple circuit control using two-phase clock pulses, the proposed converter can realize small ripple noise. Concretely, the output ripple of the proposed converter is about 7% when the output power is less than 50W. Figure 8 shows the simulated power efficiency as a function of

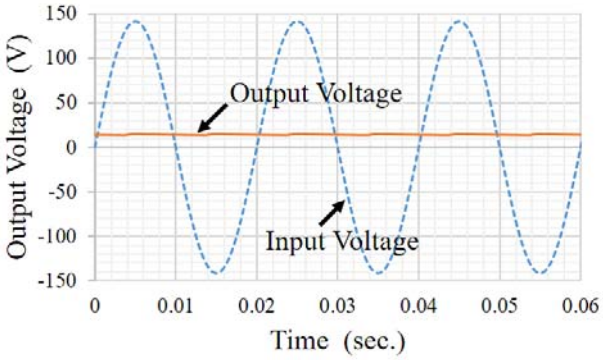


FIGURE 5. Simulated output voltage of the proposed converter when the output load is 100Ω

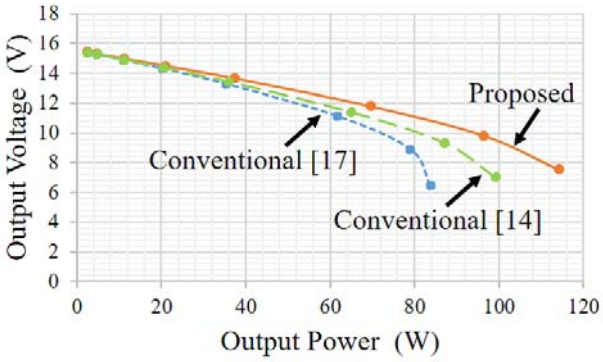


FIGURE 6. Simulated output voltages as a function of the output power

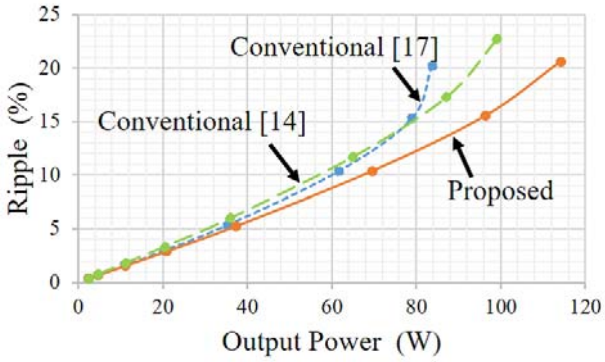


FIGURE 7. Simulated ripples as a function of the output power

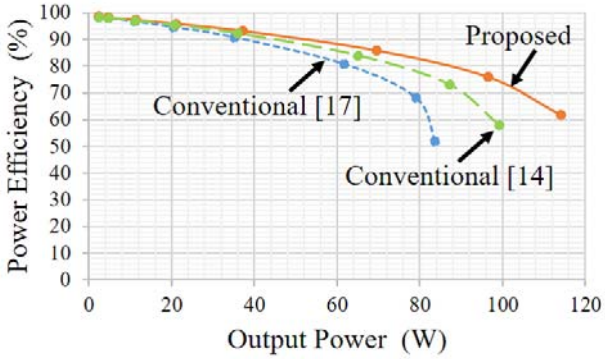


FIGURE 8. Simulated power efficiency as a function of the output power

TABLE 3. Summary of comparison results

	Size	Efficiency	Voltage drop	Ripple
Proposed converter	2	1	1	1
Conventional converter [14]	3	2	2	3
Conventional converter [17]	1	3	3	2

1: Best, 2: Middle, 3: Worst.

the output power. As you can see from Figure 8, the power efficiency of the proposed converter is higher than that of the conventional converters. The proposed converter can achieve more than 90% efficiency when the output power is less than 50W.

Table 3 shows the summary of comparison results. As you can see from Table 3, the proposed converter gives a better performance than the conventional converters.

5. **Experiments.** To clarify the feasibility of the proposed converter, experiments are performed concerning the proposed converter. Figure 9 demonstrates the experimental circuit of the proposed converter. In Figure 9, the experimental circuit was built on a breadboard by using commercially available circuit components shown in Table 4, where a small transformer was connected between the commercial power source and the experimental circuit in order to isolate the power source from the output load. In the experimental circuit, the input voltage was converted by switching photo MOS relays. To drive the photo MOS relays safely, Darlington transistor arrays were connected between the photo MOS relays and the micro controller.

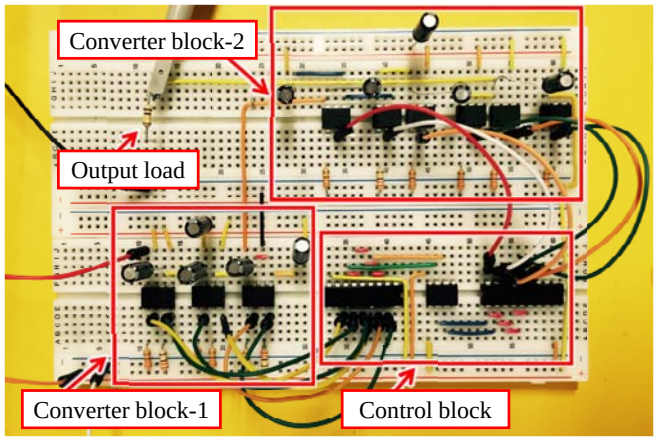


FIGURE 9. Experimental circuit of the proposed converter

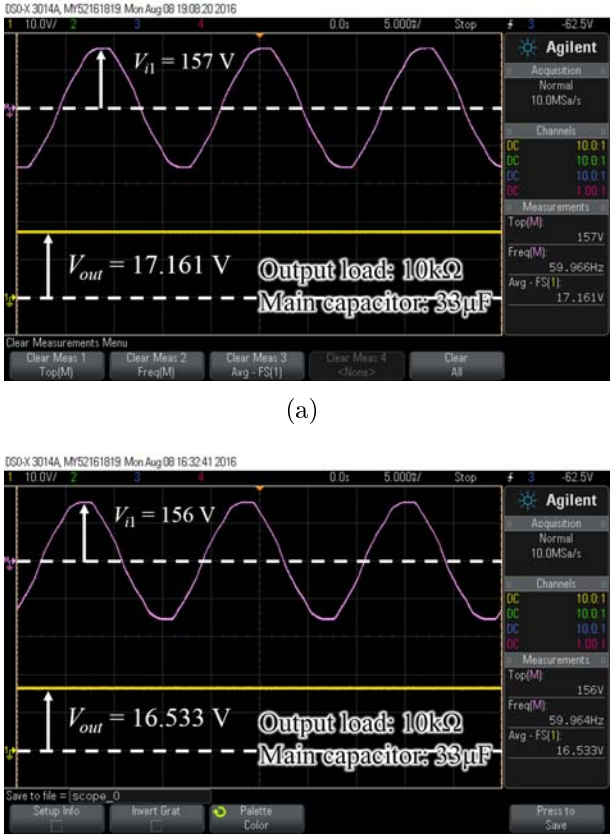
TABLE 4. Circuit components of the experimental converters

Parts	Components	Models
Full bridge circuit	Diode switch	1N4007
	Capacitor	165μF
Control block	Micro controller	PIC12F1822
	Darlington driver IC	TDG2083APG
	Current control resistance	330Ω
Converter block-1	Power switch	AQV212
	Capacitor	33μF
Converter block-2	Power switch	AQW216
	Capacitor	33μF
Output load	Resistance	10kΩ

Figure 10 demonstrates the measured output voltage when the output load is 10kΩ, where the input voltage was set to V_{in} = 141V@60Hz and the period of clock pulses was set to $T = 100\mu$s. In the experimental circuit of Figure 10, the turn ratio of the transformer between the primary side and the secondary side is 1 : 1. However, due to component fluctuations in the transformer, the turn ratio was practically 1 : 1.1. For this reason, the experimental input voltage was about 155V (141V $\times$ 1.1). As Figure 10(a) shows, the output voltage of the proposed converter is about 17.2V. On the other hand, as Figure 10(b) shows, the measured output voltage of the conventional converter reported in [17] is about 16.5V. Obviously, the proposed converter can achieve and offer higher output voltage than the conventional converter reported in [17]. Furthermore, the feasibility of the proposed converter can be confirmed by the experimental results of Figure 10.

6. **Conclusions.** For small power applications, a novel step-down SC AC-DC converter has been proposed in this paper. By connecting two converter blocks in series, an AC input is converted twice by the proposed converter. Unlike conventional converters, the proposed converter is driven by non-overlapped two-phase clock pluses, where the voltage conversion is performed by using series-connected flying capacitors.

The characteristics of the proposed converter were clarified by theoretical analysis, circuit simulations, and experiments. In the theoretical analysis, the equivalent circuit of the proposed converter was obtained by assuming a four-terminal equivalent model. From the equivalent circuit, the vital characteristics, such as power efficiency and output



(a)

(b)

FIGURE 10. Measured output voltages: (a) proposed converter and (b) conventional converter [17]

voltage, were derived. The results of the theoretical analysis showed that the proposed converter can achieve higher power efficiency and smaller voltage drop than conventional converters. The results of the theoretical analysis were verified by circuit simulations using a SPICE simulator. The SPICE simulations demonstrated that the proposed converter is superior to conventional converters in the point of power efficiency, voltage drop, and output ripple. These simulated results agreed with the results of the theoretical analysis. When the output power was less than 50W, the proposed converter achieved about 90% efficiency and 7% output ripple. Furthermore, the feasibility of the proposed converter was verified by experiments, where the experimental circuit was built with commercially available components on a breadboard. The experimental circuit provided a DC voltage by converting an AC voltage. The measured output voltage of the proposed converter was about 3.8% higher than that of the conventional converter when the output load was 10kΩ. From the results of the theoretical analysis, circuit simulations, and experiments, the proposed converter can offer not only high power efficiency but also simple control with the small number of circuit components.

As a future study, we are going to implement the proposed AC-DC converter into a hybrid IC form. Concerning the implemented converter, the detailed experiments will be conducted to clarify the properties of the proposed converter.

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