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ANALYSIS AND IMPLEMENTATION OF REVERSIBLE DUAL EDGE TRIGGERED D FLIP FLOP USING QUANTUM DOT CELLULAR AUTOMATA

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Abstract. *Reversible logic and quantum dot cellular automata (QCA) together can be considered as the most promising technologies for future generation computers. As CMOS circuits are approaching limits in minimizing area and power dissipation, reversible logic and QCA technology have potential to replace CMOS. Moreover, limited research is done on reversible sequential circuits with QCA implementation. This paper targets design and implementation of a basic sequential element, a reversible dual edge triggered D flip flop, using QCA. The logical functionality, computational and power analysis of the proposed circuit has been investigated in this work. This is one of such first attempts to design, analyze and implement reversible sequential element using QCA. This design will facilitate the conception of complex reversible sequential circuits in the area of QCA circuits.*

Keywords: Reversible logic, QCA, Power analysis, DET, Flip flop

1. **Introduction.** In today's technological era CMOS is the governing technology in very large scale integration (VLSI) systems. However, as size of the transistor is shrinking, problems like high leakage current, high lithography cost, power consumption and limitation of speed in GHz are arising. Consequently, we need some alternative technology which can substitute CMOS, prevailing better properties and performance than CMOS. One of the best feasible options is blend of reversible logic and quantum dot cellular automata (QCA). These are the emerging technologies which can be used for ultra low power nano-circuits. QCA is a unique nanotechnology which assures ultra low power, exceptionally dense and very high speed configuration for implementing any logical function at nano-scale [1]. It was first proposed by Lent et al. [2]. Moreover, Landauer proposed that classical logic circuit dissipates heat of the order KTln2 joule for each bit lost in computation, where K is Boltzmann's constant and T is absolute temperature [3]. This heat dissipation occurs in irreversible circuits and can be eliminated by introducing reversibility in the circuit [4]. Fredkin and Toffoli proposed two conservative gates that possess reversibility and ideally have zero power dissipation [5]. A lot of research has been done on reversible gates and circuits. Reversible logic circuits find numerous applications in low power VLSI, quantum computing, optical and DNA computing. Many investigations have been done on reversible combinational circuits but still there is scope to explore reversible sequential circuits. In recent years, many investigations have been reported on designs of reversible flip flops [6-12], counters [13,14], registers [15], and memory cells [16].

A quantum dot cellular automaton (QCA) is seemed to be an area of interest for many researchers in modern days. In QCA, information is stored and transmitted by formations

and polarizations of electrons in QCA cells rather than current or voltage as in case of CMOS [17-19]. After the introduction of QCA, numerous designs of combinational and sequential QCA circuits have been reported [20-24]. However, there are very few papers which describe reversible circuits with QCA implementation [25-28]. As currents and voltage levels are not utilized in QCA, the power consumption is negligible. Timler and Lent in 2002 depict power dissipation and gain in QCA cell [29]. Nevertheless, a number of studies have focused on power analysis of QCA circuits. An upper bound power dissipation model for QCA circuits was reported by Srivastava et al. [30]. First ever tool for power analysis QCApro was illustrated by Srivastava et al. [33] which brings transformation in QCA circuit analysis. Some articles demonstrated different methods of power calculation in QCA circuits [32,33]. Few research papers have reported power analysis of certain logical gates such as XOR gates using QCA circuits [34,35].

Reversible computation is known for its application in loss less computing and quantum dot cellular automaton (QCA) is known for its exceptional properties such as exceedingly high density and high operation speed with ultra-low power dissipation. Definitely merging reversibility in QCA domain will add tremendous benefits resulting in ultra low power, highly dense circuits for future generation computers. Implementation of few reversible gates such as Fredkin gate, Feynman gate and their power analysis is reported in [36] and [37]. Sequential circuits form core of the digital systems; thus in this paper authors have shown the implementation of basic building blocks of sequential circuits and their detailed analysis.

In this paper, a reversible dual edge triggered D flip flop has been carefully designed using QCA implementation. The proposed QCA D flip flop can work as a basic building block for sequential circuits.

The contributions of this paper are as follows.

1) The design of an optimized, robust reversible dual edge triggered D flip flop using positive and negative edge triggered latches is proposed. Design of these latches using reversible gates is done. The reversible gates are selected so as to have minimum garbage outputs and quantum costs.
2) Implementation of the latches and reversible flip flop using QCA is carried out. This implementation is optimized in terms of QCA cells and area. It is one of such first attempts in reversible sequential circuits. The implementation is done using standard QCA designer tool 2.0.3.
3) Objective analysis of the proposed circuits in terms of quantum parameters such as number of gates, number of cells, area, latency is carried out. This analysis will add on the configurational peculiarities of the circuit.
4) Simulation and verification of the proposed circuit are depicted to check correctness of the flip flop using QCA designer simulator.
5) Power/energy analysis of the proposed flip flop at different tunneling energies is computed.
6) The computational functionality of the proposed QCA flip flop circuit is tested using radius of effect and temperature variations.
7) The design and implementation of 4 bit reversible SIPO register are shown using the proposed DET flip flop. This register is kind of shift register which takes input serially and generates parallel output.

This research paper is explained in six sections. In Sections 2 and 3, the introductory concepts of QCA and reversible circuits are portrayed. In Section 4, design of the proposed reversible dual edge triggered D flip flop is illustrated along with its QCA implementation. Simulation results along with power and computational analysis of circuit for various

parameters are shown in Sections 5 and 6 respectively. Section 6 also describes register design and conclusion has been presented in the final section.

2. **Preliminaries.**

2.1. **QCA background.**

2.1.1. *QCA cell.* The fundamental structure in quantum dot cellular automata is a QCA cell which is a squared cell with four quantum dots placed at its corners and two free electrons. These electrons can tunnel quantum mechanically by modulating tunnel barriers between dots and assemble diagonally due to Coulombic repulsion (Lent et al. [1]). The two electronic arrangements, representing cell polarization $P = -1$ and $P = +1$, can be encoded as logic 0 and 1, respectively as shown in Figure 1.

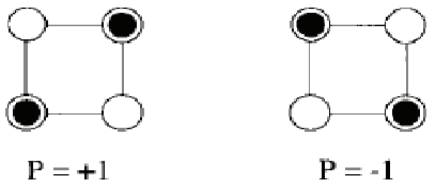

FIGURE 1. Quantum cell with polarization

2.1.2. *QCA gates.* The elementary gates in QCA design are majority gate and an inverter as shown in Figure 2. A majority gate is realized with five QCA cells with three inputs and one output. It takes input from three cells and provides decision on the fourth cell. The output is based on the majority of input cells. If majority of input cells are polarized as logic 1, then output of the gate is also 1. The majority gate realizes a three-variable logic function as follows.

$$\mathrm{M(A, B, C)} = \mathrm{AB} + \mathrm{AC} + \mathrm{BC} \tag{1}$$

Equation (1) represents the basic Boolean expression for majority gate, using which essential functions like logical AND and logical OR can be implemented by fixing one input to logic 0 or 1, respectively. Another fundamental gate is inverter as shown in Figure 3. If the cells are placed at 45° then output is complement of the input realizing an inverter. This way all the basic gates and hence universal gates can be implemented using majority gates and QCA inverter.

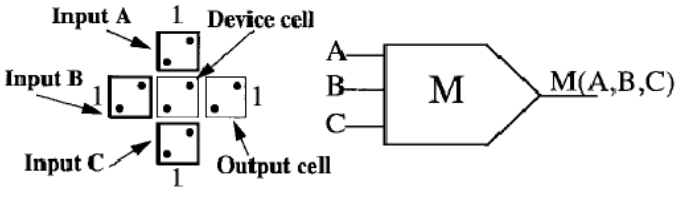

FIGURE 2. Majority gate

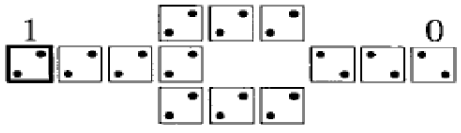

FIGURE 3. QCA inverter

2.1.3. *QCA clocking scheme.* Direction of data flow in a QCA circuit is governed by clock signals. To ensure QCA circuits close to a ground state, adiabatic switching is the extensively used clocking technique. An adiabatic periodic clock signal has four different phases: switch, hold, release, and relax. The clock signal affects the tunnel barriers between the dots, alternately prohibiting or allowing the electrons to tunnel. In these four phases: switch, hold, release, and relax, the clock signal influences the tunnel barriers between the dots, resulting in raising or lowering of the barriers. In turn the movement of electrons in the cell is controlled which affects the polarization of cell as shown in Figure 4.

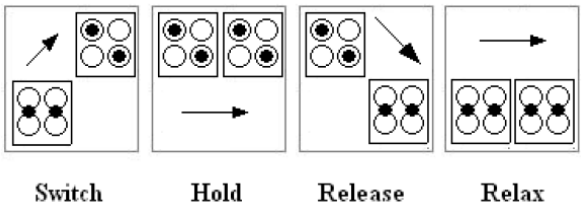

FIGURE 4. Clock phases in QCA

A switch phase alters the polarization of the cell according to the driver cell, hold phase seizes the state of polarization, release phase releases the state of polarization and relax phase ensures the null polarization. The resultant outcome is that the information is latched while moving from one clock zone to the other [18].

3. **Reversible Logic.**

3.1. **Reversible gates.** Reversible logic gates have equal number of inputs and outputs and have bijective mappings between input vectors and output vectors; consequently the input data can be recreated from the output vector states [4]. A reversible gate with n inputs and n output is known as $n * n$ gate.

A. Feynman gate. Feynman gate is a $2 * 2$ reversible gate shown in Figure 5. It is also known as CNOT, i.e., controlled NOT Gate [5]. The input (A, B) and output (P, Q) relation is as follows.

$$\begin{aligned} \mathrm{P} &= \mathrm{A}; \\ \mathrm{Q} &= \mathrm{A} \text{ xor } \mathrm{B} \end{aligned}$$

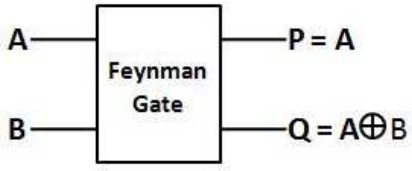

FIGURE 5. Feynman gate

B. Fredkin gate. Fredkin gate is a $(3*3)$ conservative reversible gate as shown in Figure 6 [5]. The relation between input vectors and its output vectors is as follows.

$$\begin{aligned} \mathrm{P} &= \mathrm{A}; \\ \mathrm{Q} &= \bar{\mathrm{A}}\mathrm{B} + \mathrm{AC}; \\ \mathrm{R} &= \mathrm{AB} + \bar{\mathrm{A}}\mathrm{C} \end{aligned}$$

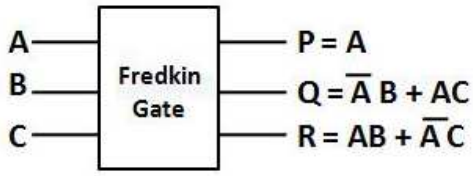

FIGURE 6. Fredkin gate

4. Proposed Design Approach.

4.1. Reversible dual edge triggered D flip flop. Dual edge triggered (DET) flip flop is designed here using two D latches, namely positive edge triggered latch and negative edge triggered latch and a multiplexer. For designing the proposed reversible DET flip flop, reversible gates such as Fredkin gate and Feynman gate are used. Figure 7 illustrates the structure of the proposed reversible DET flip flop. Two pairs of Fredkin and Feynman gates constitute two parallel opposite level sensitive flip-flops (D latches) with a third Fredkin gate as a multiplexer. The output of negative edge triggered latch is X and that of positive edge triggered latch is Y. Both the outputs are applied to the third Fredkin gate which is acting as a multiplexer. G1, G2 and G3 are garbage outputs. When CLK = 0 (leading edge), the upper latch receives input D, and then the multiplexer selects and outputs the data. When CLK = 1 (trailing edge), lower latch receives input D and multiplexer selects and outputs data. This way DET flip flop generates D at the output at both the edges of the clock.

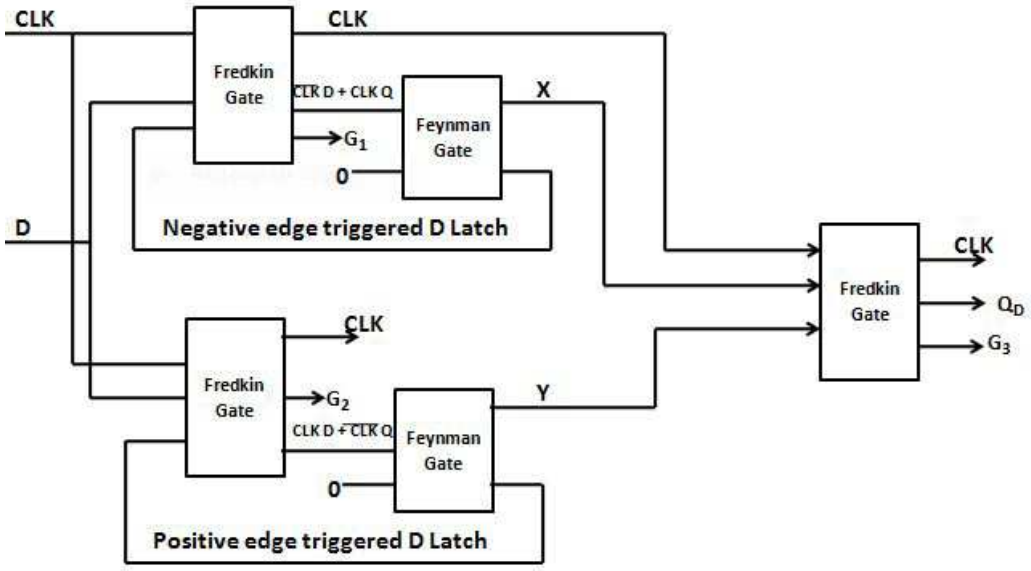

FIGURE 7. Reversible dual edge triggered D flip flop

4.2. Realization of reversible DET D flip flop using majority gates. More often QCA circuits are designed using elementary components such as majority gates. The proposed DET consists of Fredkin gate, Feynman gate and inverter which can be designed using majority gates. Figure 8 illustrates the proposed design. Conventional DET flip flop utilizing QCA is reported in [23,24] but its reversible configuration is not found in literature. This is the first attempt of its kind to realize, low power and high performance reversible DET D flip flop using QCA.

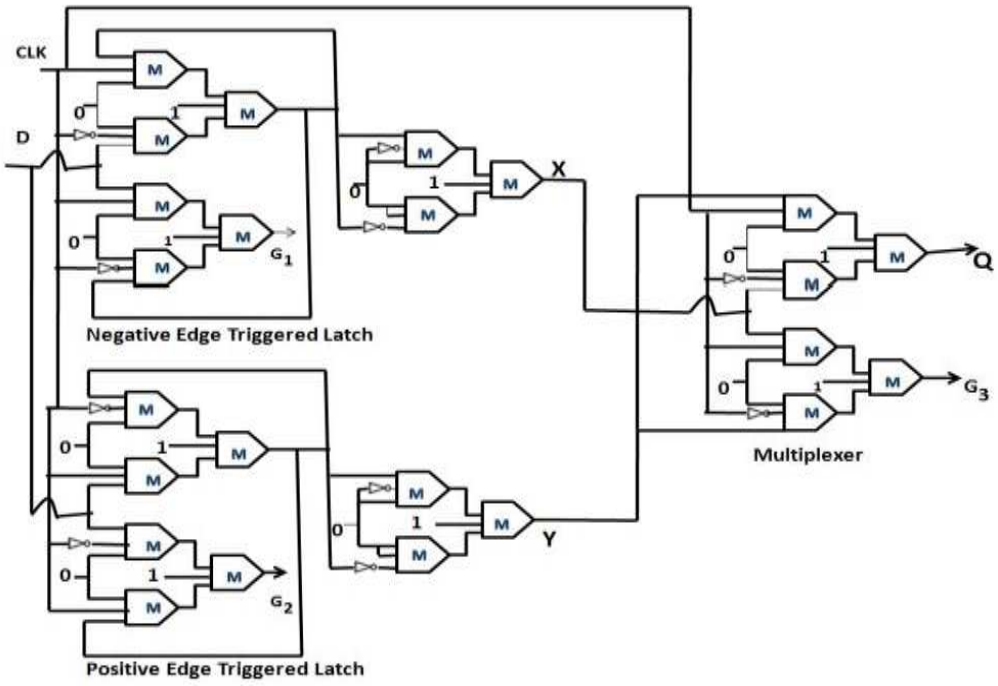

FIGURE 8. Reversible DET D flip flop using majority

4.3. **QCA implementation of reversible DET D flip flop.** DET flip flop samples data on both edges of the clock pulse and accordingly it operates at double clock frequency with more throughput than its SET (single edge triggered) counterpart. Consequently it is considered as high performance flip flop in terms of data throughput. In this paper, the intended circuit is carefully implemented using QCA and its functionality is verified using the QCA designer tool. Here Figure 9 illustrates QCA implementation using majority voters and Figure 10 shows the QCA implementation using the different approach. In the circuit of Figure 10 Fredkin gate is designed using majority gates, inverters and Feynman gate is designed using XOR structure reported in [20]. Here as the Feynman gate is designed using XOR structure of [20], the required number of majority gates is less so the circuit is even compact. The proposed QCA implementations of reversible DET are obtained with QCA designer 2.0.3. In Figure 9, left half represents negative edge triggered latch while right half is positive edge triggered latch. In Figure 10, D and CLK are the inputs applied. Upper half of the circuit represents negative edge triggered D latch and lower half shows positive latch. X and Y represent outputs of negative and positive latches respectively. Right half of the circuit is Fredkin gate acting as a multiplexer which is selecting outputs from both latches. Q corresponds to the final output of DET D flip flop while G1, G2 and G3 indicate garbage outputs.

4.4. **Structural analysis.** Any QCA circuit is scrutinized on the basis of numerous QCA parameters. Table 1 shows the structural analysis of the proposed design in terms of the various QCA parameters such as number of majority voters, the number of QCA cells, the number of inverters, circuit density, and the number of clocking zones used to design the circuit. This analysis provides insight of area, clock latency and compactness of the circuit. Table 1 illustrates the analysis of Figures 9 and 10 and indicates that the structure in Figure 9 requires more clock cycles and more latency while the structure in Figure 10 needs comparatively lesser QCA cells and clock latency. Feynman gate used in Figure

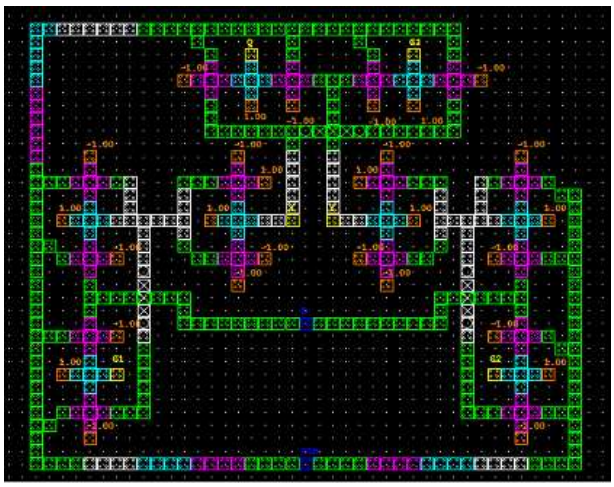

FIGURE 9. QCA implementation of reversible DET D flip flop with majority voters

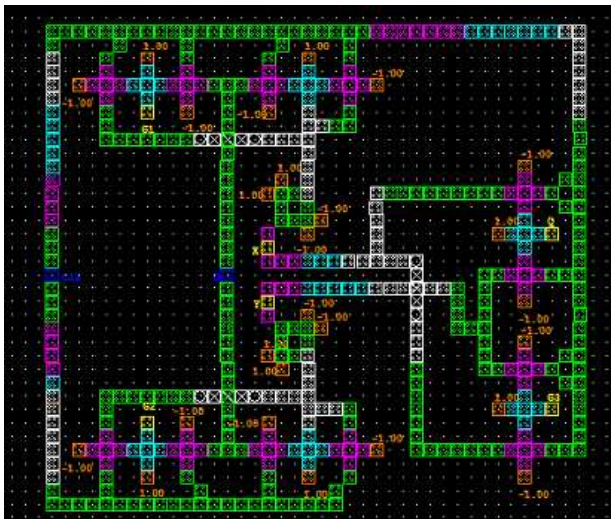

FIGURE 10. QCA implementation of reversible DET D flip flop using XOR structure reported in [20]

10 is not constituted using majority gate, inverter and hence needs less number of QCA cells.

5. **Analysis of Simulation Results.** In many applications such as registers, counters, memories, DET flip flops are used to increase throughput at the same frequency. Figure 11 illustrates the simulation results of the proposed reversible DET D flip flop to prove correctness of the circuit. The simulation results are verified with the intended values of DET D flip flop on QCA Designer 2.0.3. Figure 11 implicates D and CLK as input waveforms and X, Y and Q as outputs of negative edge triggered, positive edge triggered latches and DET flip flop respectively.

At the input, when CLK edge is trailing, the output X = D (output of negative edge triggered latch) and Y = previous output, subsequently when CLK edge is rising then X = previous output and Y = D (output of negative edge triggered latch).

The output is delayed due to clock latency which is indicated in the waveform. The multiplexer output Q selects X when clock is trailing and selects Y when clock is rising. Thus waveform Q illustrates that DET output is following input D even at falling edge

TABLE 1. Structural analysis of reversible dual edge triggered D flip flop

	QCA circuits	No. of majority voters	No. of QCA cells	No. of inverters	Total area in μm^2	Latency (Clock)
DET using Feynman gate (XOR structure) of [20] (Figure 10)	Feynman gate	–	15	–	0.02	1
	Fredkin gate	6	55	2	0.07	1
	Reversible pos/neg edge triggered latch	6	99	2	0.14	1.5
	Reversible DET D flip flop	18	465	6	0.58	3
DET using Feynman gate with majority gates (Figure 9)	Feynman gate	3	31	1	0.04	1
	Fredkin gate	6	76	2	0.07	1
	Reversible pos/neg edge triggered latch	9	116	3	0.16	2
	Reversible DET D flip flop	24	475	8	0.57	4

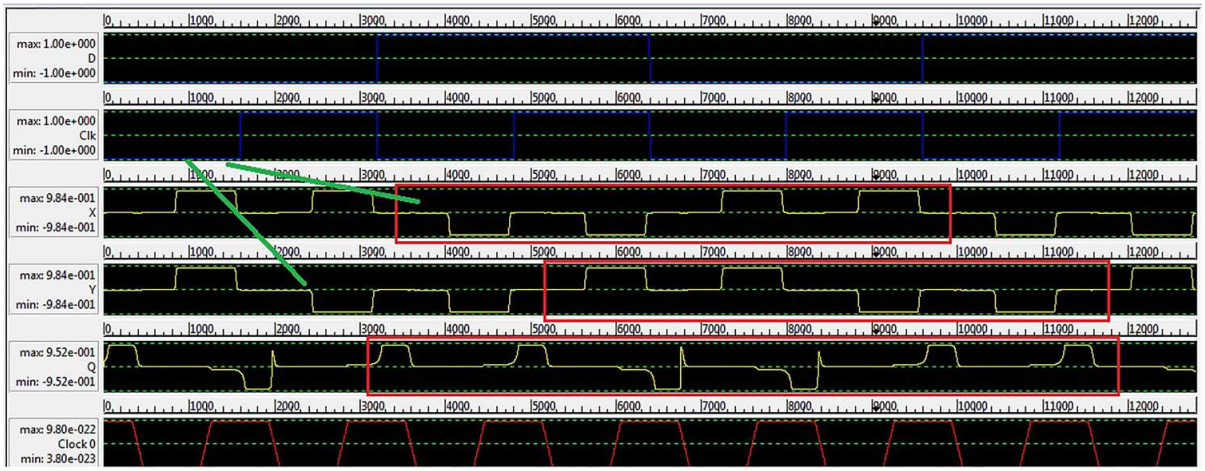

FIGURE 11. Simulation results of reversible DET D flip flop

and at rising edge. Therefore, the circuit functions capably and thus can be used in various sequential circuits as a building block.

6. **Power and Computational Analysis.**

6.1. **Estimation of power dissipation in the proposed QCA circuit.** The most precise power dissipation model has been anticipated by Timler and Lent [29]. Recently, a new power estimation tool, QCAPro has been launched by Srivastava which uses upper bound model of power dissipation [30,31]. Sheikhfaal et al. [34] illustrated energy dissipation of five input majority gates, at temperature $T = 2$ °K and at different tunneling energies such as 0.25 Ek and 0.5 Ek using this tool. There are a number of approaches found in literature to calculate energy dissipation in QCA structures [32]. Liu et al. [33] demonstrated that the power dissipation model for every QCA cell is analogous; consequently, the net power in a circuit for one clock cycle can be obtained by totaling the power used by each cell. At length, it is worth mentioning that the power consumption of a cell has static and dynamic parts [33]. Also, the power consumption of QCA circuit is dependent on the logic gates used in designing the circuit. Use of a greater number

of logic gates, i.e., the majority gate and inverter, implies higher power dissipation by the QCA circuits. Power dissipation of inverter, majority gate is estimated by Liu et al. using a concept of Hamming distance. Hamming distance of two inputs $X1$ and $X2$ is the Hamming weight (HW) of $X1$ xor $X2$, where HW is the number of binary "1"s. HD($X1$, $X2$) = HW($X1$ xor $X2$). Liu et al. [33] reported that due to variation in the Hamming distance between inputs to the QCA circuit, the power dissipation will also be altered. For example, if input changes 0→0 or 1→1, in inverter, indicates Hamming distance '0', and for this dissipated power is 0.8 meV at $\gamma = 0.25$ Ek and 8.0 meV at $\gamma = 1.0$ Ek. For 0→1 or 1→0 input change in polarization, Hamming distance '1' is considered for the inverter and then the estimated dissipation will be 28.4 meV at $\gamma = 0.25$ Ek and 30.2 meV at $\gamma = 1.0$ Ek. Similar estimation is done for majority gate as well [33].

Recently, estimation of energy dissipation has been done for QCA layouts of parity generator and presented at temperature $T = 2$ °K and at different tunneling energies such as 0.25 Ek, 0.5 Ek, 0.75 Ek and 1 Ek (Das et al. [36]). Similar estimation has been done for Fredkin gate and user authentication circuit [37].

Using the similar approach, evaluation of power is done for the proposed circuit which is shown in Table 2. Feynman gate implementation in QCA requires 3 majority gates and one inverter out of which two majority gates have two fixed inputs hence HD is taken as '1' and the third majority gate has only one fixed input hence HD is considered as '2'. In case of inverter, it has a variable input and hence its HD is '1'. Assuming the values given in [31] as a reference, the power dissipation for various circuit blocks is estimated as shown in Table 2 for different tunneling energies.

Table 2. Power dissipation in the proposed circuits

Proposed QCA circuits	Power dissipated at $T = 2$ °K (in meV)			
	0.25 Ek	0.5 Ek	0.75 Ek	1 Ek
Feynman gate	58.4	63.4	70.9	79.6
Fredkin gate	208.6	215.6	226.6	239.2
Reversible positive/negative edge triggered D latch	267	279	297.5	318.8
Reversible DET D flip flop	742.6	773.6	821.6	876.8

Graphical illustration of this energy dissipation is as shown in Figure 12. The graph depicts that power (energy) dissipation values for Feynman gate and Fredkin gate are very less and are slightly increasing with increase in tunneling energy. For reversible DET D flip flop, the energy consumed is low as it is in the range of 742 meV to 876 meV, i.e., around 1.1895e-19 Joules to 1.4046e-19 Joule.

6.2. **Temperature dependency of output polarization.** Mean output polarization of the output X (from negative edge triggered latch), Y (from positive edge triggered latch), Q of reversible DET D flip flop at different temperatures is obtained on QCA designer using coherence vector engine and plotted as shown in Figure 13. It shows that after 10 °K the value of mean polarization for Q starts reducing while outputs from both the latches retain till 16 °K. Hence the proposed QCA circuit can produce desired output within a temperature range of 1 °K to 10 °K.

Mean polarization is evaluated by taking average of maximum and minimum polarization values. For example, maximum and minimum polarization values for output Q are 9.69e-01 and −9.68e-01; thus mean polarization comes out to be 9.685e-01.

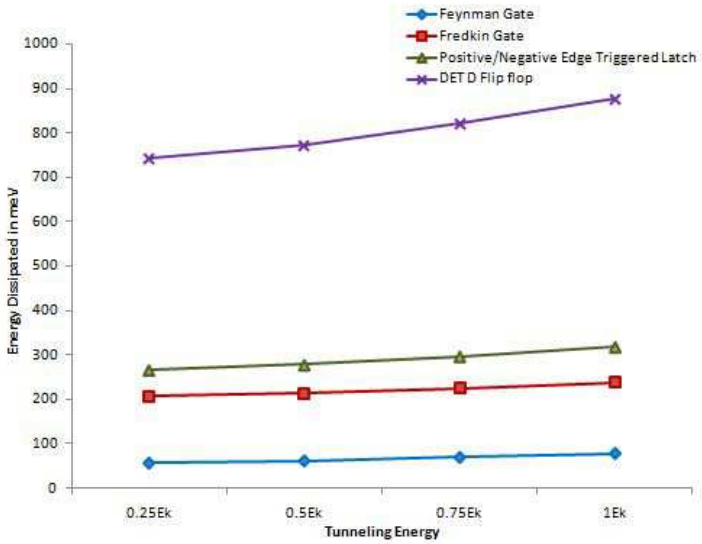

FIGURE 12. Power dissipation analysis of the proposed QCA circuit

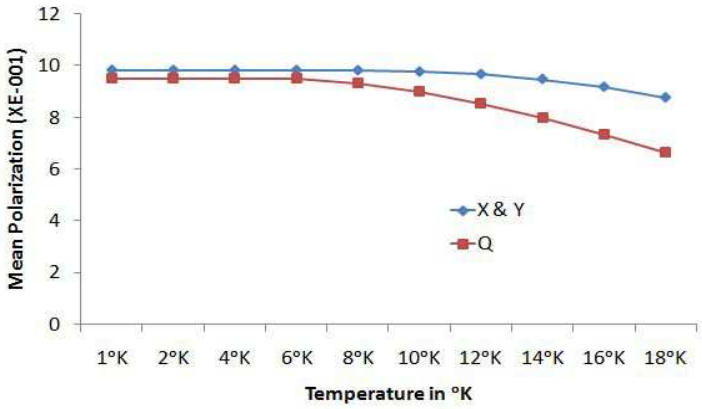

FIGURE 13. Mean polarization versus temperature

6.3. **Cell interaction and cell alignment.** Important constraint in QCA circuit is the radius of effect of a cell; it is the radius at which the cell interacts with adjacent cells. The radius of effect is measured from centre of one cell to the centre of another.

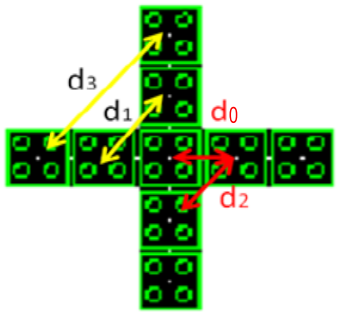

FIGURE 14. Radius of effect

As shown in Figure 14, the radius of effect can be obtained by considering following relations.

$$d_0 = w + s, \quad d_1 = \sqrt{2}d_0, \quad d_2 = \sqrt{5}d_0, \quad d_3 = \sqrt{8}d_0$$

where d is the radius of effect, w is the width of the cell and s is the distance of separation. Hence, the radius of effect for the second (d_1), third (d_2) and fourth (d_3) nearest neighbor will be as given in equations. With $w = 18$ nm, $s = 2$ nm, the different values of d are given in Table 3.

TABLE 3. Relation between Radii of neighbor cells

Radius of effect	Relation	Value in nm
d_0	$d_0 = w + s$	20
d_1	$d_1 = \sqrt{2}d_0$	28.28
d_2	$d_2 = \sqrt{5}d_0$	44.72
d_3	$d_3 = \sqrt{8}d_0$	56.56

The deviation in the output polarization of the proposed reversible D flip flop with respect to the variation in radius of effect is shown in Table 4.

TABLE 4. Deviation of output polarization due to radius of effect

Radius of effect (nm)	Polarization of output X & Y	Polarization of output Q
20	Failed	Failed
28.28	9.87e-001	9.51e-001
44.72	9.84e-001	9.53e-001
56.56	9.84e-001	9.52e-001
72.11	9.84e-001	9.52e-001
84.85	9.84e-001	9.53e-001

It can be observed from the above table that when radius of effect is kept beyond 20 nm, the output polarizations give correct values but at 20 nm output polarizations fail.

6.4. **Serial in parallel out register using the proposed DET flip flop.** The proposed QCA circuit of reversible DET can be used to construct numerous sequential circuits.

One of such circuits, reversible serial in parallel out shift register is carefully designed using the proposed DET and illustrated in Figure 15. The circuit is 4 bit SIPO shift register with input D applied to the first flip flop and 4 outputs Q1, Q2, Q3, Q4 taken from all the flip flops. Simulation and computational analysis of this circuit can be done in a future work.

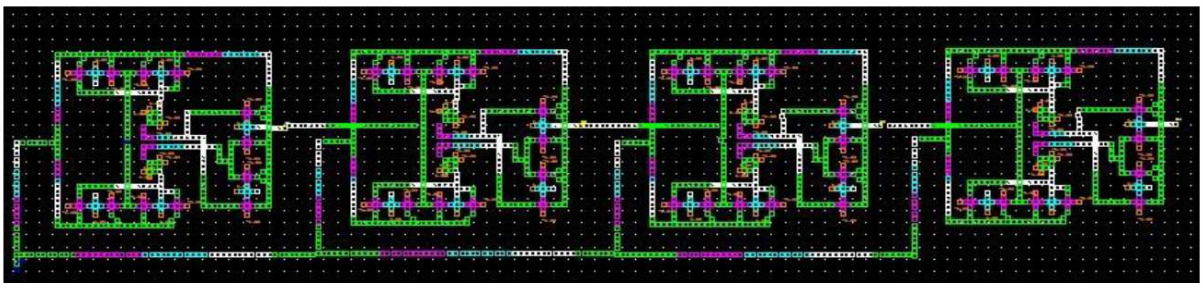

FIGURE 15. QCA implementation of reversible SIPO register using proposed reversible DET

6.5. **Result discussion.** This paper demonstrates the complete design as well as objective analysis of the proposed QCA circuit. Simulations confirm the precision of DET D flip flop. Further energy/power analysis exemplifies the ultra low power dissipation in the proposed circuit which is of the order of 700 to 800 meV. This shows potential of such circuits in future technology as alternative of CMOS. Moreover, the circuit is studied for temperature variations (1 °K to 10 °K) and variation in radius of effect (range of 28 nm to 84 nm) which predicts exact parameters at which circuit can perform consistently.

7. **Conclusion.** This research paper explores design, QCA implementation and analysis of reversible dual edge triggered D flip flop which is one of the inevitable and crucial building blocks of reversible sequential logic design. The design is scrutinized for various parameters such as the number of majority voters, the number of cells, area, and latency and is verified on QCA designer tool. This research paper has also exhibited the power estimation of the proposed QCA circuit. The circuit is carefully studied for temperature dependency, robustness and deviation in polarization due to variation in radius of effect. Application of the proposed flip flop is also shown by implementing reversible SIPO register using QCA. This design and implementation of reversible DET D flip flop using QCA are one of such first attempts and a decisive step towards the target of ultra low power digital design in nanotechnology using reversible logic.

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