

A WIDE RANGE MANHATTAN DISTANCE SEARCH CIRCUIT USING NEURON CMOS INVERTERS

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ABSTRACT. *Recently, an associative memory has been studied actively. In the associative memory, not only matched data but also similar data are searched fast. The associative memory is expected for realizing as image recognition and malware detection that require to process vast information, because it can search for the most similar data to the input data at high-speed in fully parallel. A neuron complementary metal-oxide-semiconductor (CMOS) inverter is an electronic element expected to be highly functional and integrated for an integrated circuit (IC) as “soft-hardware” which is constituted by changing a conventional MOS transistor slightly. In this paper, we will report the design of a wide range Manhattan distance search circuit utilizing the neuron CMOS inverters which is a vital component in the associative memory. The proposed circuit can retrieve all data within the specified Manhattan distance from outside, and can process more flexible than the most similar data searching. Furthermore, the proposed circuit can eliminate influences of the variation of threshold voltage and initial charge of the neuron CMOS inverters which are problems in conventional circuits. Through simulations using a 0.18 μ m CMOS process of Rohm Semiconductor with HSPICE, we confirmed an expected characteristic of the proposed circuit.*

Keywords: Manhattan distance, Associative memory, Neuron CMOS inverter, Time domain

1. **Introduction.** Recently, an associative memory has been collecting a lot of attention and has been studied actively according to the development of information technologies [1-4]. In addition to a conventional memory function, the associative memory has a feature which can retrieve the most similar data from a database at high speed. For this reason, it is expected that the associative memory can be applied to malware detection, data compression, image processing and pattern recognition [5,6]. The similarity between input data and reference data is expressed by the distance such as the Hamming distance and the Manhattan distance [7-9]. For example, the Hamming distance is used for fingerprint recognition and character recognition. On the other hand, the Manhattan distance is used for color image recognition and data compression. In past studies, some researchers

have proposed a digital type associative memory and a method of converting the distance to the time domain, etc. However, the associative memory has not been practical yet, because there are some problems such as searching speed and power consumption.

To solve these problems, by utilizing the neuron complementary metal-oxide-semiconductor (CMOS) inverters, some challenges have been tackled [10,11]. However, these conventional circuits have problems. It is that the circuits cause a malfunction by the influence of the variation of the threshold voltage of the neuron CMOS inverters with manufacturing and temperature. Furthermore, the circuit of [11] is affected by the initial charge of the floating gate of the neuron CMOS inverter.

The authors have already proposed a minimum Manhattan distance search circuit using neuron CMOS inverters which is an important functional circuit of the associative memory [12]. The minimum Manhattan distance search circuit can retrieve the most similar data at high speed. The neuron CMOS inverter proposed by Shibata and Ohmi is an electronic element which is similar to a brain neuron [13]. This element is constituted by modifying a general MOS transistor slightly and is expected to be a high-function and high-integration circuit as a “soft-hardware”. Utilizing the neuron CMOS inverters, the proposed minimum Manhattan distance search circuit converts the Manhattan distance to the floating gate voltage of the neuron CMOS inverter. Then, the floating gate voltage is converted to a time. By these operations, the proposed circuit can retrieve matching data as well as the most similar data in a parallel manner.

The associative memory with the wide range searching is expected to obtain more flexibility for information processing [14]. In this paper, we propose a wide range Manhattan distance search circuit using the neuron CMOS inverters by modifying the minimum Manhattan distance search circuit. The proposed circuit can retrieve all data within the specified Manhattan distance from outside. Furthermore, the proposed circuit can eliminate the influences of the variation of threshold voltage and initial charge of the neuron CMOS inverters by connecting the floating gate to the output terminal of the neuron CMOS inverter before searching operation. In this study, we design the proposed wide range Manhattan distance search circuit by assuming an ROHM Semiconductor $0.18\mu\text{m}$ CMOS process. Furthermore, we clarify the characteristics of the proposed circuit by the HSPICE simulation.

The rest of this paper is organized as follows. In Section 2, the circuit configuration of the wide range Manhattan distance search circuit which is further developed from the minimum Manhattan distance search circuit is analyzed. In Section 3, the HSPICE simulations of the proposed circuit are presented. In Section 4, conclusion of this paper is drawn. Furthermore, future study is described.

2. Circuit Configuration. Figure 1 illustrates the circuit configuration of the wide range Manhattan distance search circuit using neuron CMOS inverters. The equivalent circuit of Figure 1 is expressed by Figure 2. An input data and a reference data consist of N bits \times M elements when the number of words is L . In this figure, the input data and the reference data are expressed as $A_j = (a_1, \dots, a_i, \dots, a_N)$ ($(j = 1, 2, \dots, M)$ and $(i = 1, 2, \dots, N)$) and $B_{j,k} = (b_{1,j,k}, \dots, b_{i,j,k}, \dots, b_{N,j,k})$ ($(k = 1, 2, \dots, L)$), respectively. Here, A_j and $B_{j,k}$ are binary data, and $\mathbf{A} = (A_1, \dots, A_j, \dots, A_M)$ and $\mathbf{B}_k = (B_{1,k}, \dots, B_{j,k}, \dots, B_{M,k})$ are vectors constituted by these M elements. $SP_j = (sp_{1,j}, \dots, sp_{i,j}, \dots, sp_{N,j})$ is the control signal for specifying the search range of Manhattan distance and is inputted binary data of search range of Manhattan distance. $\mathbf{SP} = (SP_1, \dots, SP_j, \dots, SP_M)$ is a vector constituted by these M elements. V_{DD} is supply voltage. F is control voltage to start the search operation. D_{Manh} is a sum of the absolute value of the differences between the elements A_j and $B_{j,k}$ of the input data and the reference data,

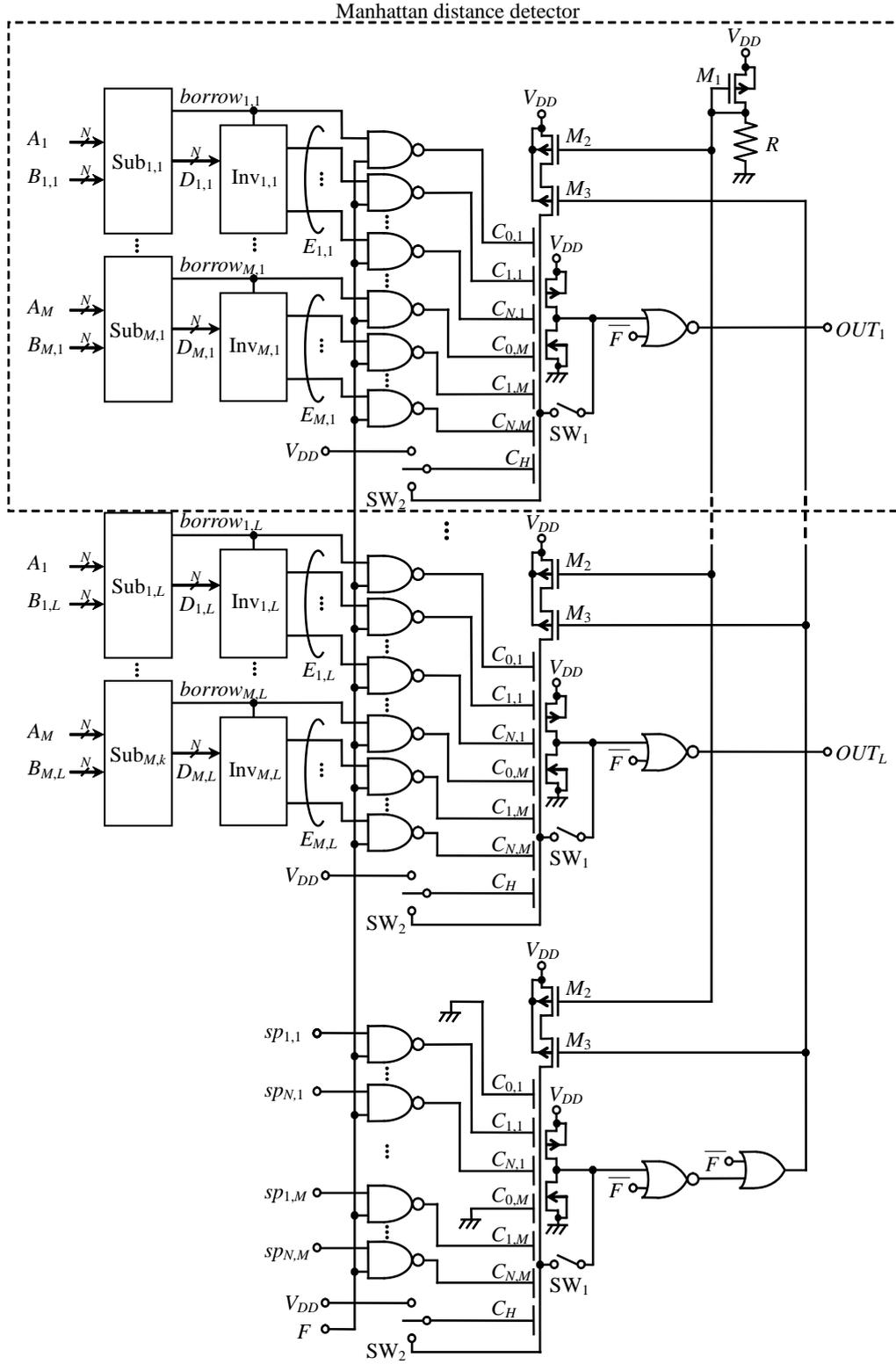


FIGURE 1. Circuit configuration of the wide range Manhattan distance search circuit

and is defined as follows:

$$D_{Manh} = \sum_{j=1}^M |A_j - B_{j,k}|. \quad (1)$$

gate are designed as follows:

$$C_{0,j} = C, \quad (2)$$

$$C_{i,j} = 2^{i-1}C, \quad (3)$$

$$\text{and } C_H = C, \quad (4)$$

where C denotes a unit capacitance. In Figures 1 and 2, $Sub_{j,k}$ is a circuit which outputs the subtraction result $D_{j,k}$ between A_j and $B_{j,k}$. The subtraction result $D_{j,k}$ is expressed as:

$$D_{j,k} = A_j - B_{j,k}. \quad (5)$$

When the result is positive, $Inv_{j,k}$ outputs the signal as it is. On the other hand, when the result is negative, $Inv_{j,k}$ outputs inversion of $D_{j,k}$. The output of $Inv_{j,k}$ $E_{j,k}$ is shown as follows:

$$E_{j,k} = \begin{cases} D_{j,k} & (D_{j,k} \geq 0) \\ \bar{D}_{j,k} & (D_{j,k} < 0). \end{cases} \quad (6)$$

For these operations, $Sub_{j,k}$ and $Inv_{j,k}$ calculate $|A_j - B_{j,k}|$. Incidentally, it needs to invert the subtraction result $D_{j,k}$ and add 1 when $A_j - B_{j,k}$ is negative. However, the proposed circuit achieves that the adder circuit is unnecessary by connecting $borrow_{j,k}$ to the neuron CMOS inverter.

Next, we will describe the operation principle of the proposed circuit. The floating gate voltage V_F of the neuron CMOS inverter is expressed by the following equation:

$$V_F = V_{TH}, \quad (7)$$

where the control voltage F is set to a low level, switch SW_1 becomes ON, and SW_2 is connected to the lower side. The amount of change in the voltage V_F , ΔV_F , is expressed by the following equation:

$$\Delta V_F = \frac{C_x}{C_T} \Delta V, \quad (8)$$

where the voltage of input terminal which has the capacitance C_x between the input terminal and the floating gate of neuron CMOS inverter changes by ΔV_F . In (8), the capacitance C_T is the total capacitance between the input terminal and the floating gate of neuron CMOS inverter and is expressed as:

$$C_T = \sum_{j=1}^M \left(C_{0,j} + \sum_{i=1}^N C_{i,j} \right) + C_H + C_P. \quad (9)$$

In (9), C_P is parasitic capacitance between the input terminal of the neuron CMOS inverter and the substrate. From (8), the floating gate voltage V_F of the neuron CMOS inverter is rewritten as follows:

$$V_F = V_{TH} + \frac{C_H}{C_T} (V_{DD} - V_{TH}), \quad (10)$$

where SW_1 turns ON and SW_2 is connected to the upper side. From (10), it proves that the output voltage of neuron CMOS inverter becomes a low level. The output $V_{i,j,k}$ and $V_{0,j,k}$ of NAND change from a high level to a low level by setting F to a high level if the input data A_j does not agree with $B_{j,k}$; that is, the i -th bit $e_{i,j,k}$ and $borrow_{j,k}$ are at a high level. In this case, the floating gate voltage V'_F is given by the following from (8) and (10):

$$V'_F = V_{TH} + \frac{C_H}{C_T} (V_{DD} - V_{TH}) - \sum_{j=1}^M \left\{ \frac{C_{0,j}}{C_T} (V_{DD} - V_{0,j}) + \sum_{i=1}^N \frac{C_{i,j}}{C_T} (V_{DD} - V_{i,j}) \right\}. \quad (11)$$

By substituting (2), (3), and (4) into (11), V'_F is expressed as:

$$\begin{aligned} V'_F &= V_{TH} + \frac{C}{C_T} (V_{DD} - V_{TH}) - \sum_{j=1}^M \left\{ \frac{C}{C_T} (V_{DD} - V_{0,j}) + \sum_{i=1}^N \frac{2^{i-1}C}{C_T} (V_{DD} - V_{i,j}) \right\} \\ &= V_{TH} + \frac{C}{C_T} (V_{DD} - V_{TH}) - \sum_{j=1}^M |A_j - B_j| \frac{C}{C_T} V_{DD}. \end{aligned} \quad (12)$$

Furthermore, the above-mentioned equation is rewritten as the following equation from (1):

$$V'_F = V_{TH} + \frac{C}{C_T} (V_{DD} - V_{TH}) - D_{Manh} \frac{C}{C_T} V_{DD}. \quad (13)$$

The output of the neuron CMOS inverter becomes a high level and the output OUT_k does not change from a low level, because V'_F is lower than the threshold voltage V_{TH} . As we can see from (13), the floating gate voltage V_F decreases in proportion to the Manhattan distance D_{Manh} . Here, V'_F decreases for 1 Manhattan distance when $borrow_{j,k}$ is in a high level. Therefore, the circuit for adding 1 to the inverted value $E_{j,k}$ is unnecessary when $A_j - B_{j,k}$ is a negative value. If 1 or more Manhattan distance is inputted to the control signal \mathbf{SP} of the Manhattan distance detector for the specifying range of the Manhattan distance, the floating gate voltage of the neuron CMOS inverter decreases in proportion to the Manhattan distance and the output of OR circuit becomes a low level. Thereby, the MOS transistor M_3 becomes ON, and the constant current flows to all floating gates of the Manhattan distance detector from the current mirror circuit constituted by M_1 , M_2 , and R . Thus, the floating gate voltage of the neuron CMOS inverter increases linearly from V'_F . The output OUT_k of the Manhattan distance detector becomes a high level when the floating gate voltage exceeds the threshold voltage V_{TH} of the neuron CMOS inverter. The time T taken from the control voltage F which becomes a high level to the output OUT_k which becomes a high level is expressed as follows:

$$T = \frac{C_T (V_{TH} - V'_F)}{I}, \quad (14)$$

where I denotes the constant current which flows through the MOS transistor M_3 . By substituting (13) into (14), T is expressed as

$$T = \frac{C_T \left\{ V_{TH} - V_{TH} - \frac{C}{C_T} (V_{DD} - V_{TH}) + D_{Manh} \frac{C}{C_T} V_{DD} \right\}}{I}. \quad (15)$$

Furthermore, by simplifying the equation, the time T is expressed as

$$T = D_{Manh} \frac{C}{I} V_{DD} - \frac{C}{I} (V_{DD} - V_{TH}). \quad (16)$$

As (16) shows, the time T is not affected by the parasite capacitances and the initial charge of the neuron CMOS inverters. Also, the time lag ΔT , which has difference 1 Manhattan distance, is expressed as

$$\Delta T = \frac{C}{I} V_{DD}. \quad (17)$$

As we can see from (17), the change of the threshold voltage V_{TH} does not affect the time lag against the difference of the Manhattan distance.

When the output of the Manhattan distance detector for specifying the range of the Manhattan distance which becomes a high level, the MOS transistor M_3 becomes OFF and the charging to the floating gate is stopped. The time taken from the output of the

Manhattan distance detector for specifying the range of the Manhattan distance which becomes a high level is in proportion to the Manhattan distance inputted the control signal SP . Because the Manhattan distance detector converts the Manhattan distance to a time, the OUT_k of the Manhattan distance detector which has the reference data within the specified Manhattan distance becomes a high level.

For these operations, the proposed wide range Manhattan distance search circuit can retrieve all reference data within a specified Manhattan distance by SP .

3. Simulation. To clarify the characteristics of the proposed wide range Manhattan distance search circuit with 4-bits, 2-elements, and 8-words, simulations were conducted by using HSPICE of Synopsis. In these simulations, a $0.18\mu\text{m}$ CMOS process of ROHM Semiconductor was assumed. In addition, the supply voltage V_{DD} was set to 1.8V, and the threshold voltage V_{TH} of the neuron CMOS inverter was designed to be 0.9V which is a half of the supply voltage V_{DD} .

Figure 3 demonstrates the simulated results when the reference data have 1-16 Manhattan distance. As we can see from this figure, the floating gate voltage V_F decreases in proportion to the Manhattan distance and then increases linearly by the current mirror circuit after the control voltage F is set to a high level. Figure 4 shows the graph of the floating gate voltage V_F immediately after the control voltage F is set to a high level. In this figure, it can be seen that the floating gate voltage V_F of the neuron CMOS inverter νCMOS decreases in proportion to the Manhattan distance. The simulated result of Figure 4 satisfies (13). Figure 5 shows the graph of the time that the floating gate voltage of the Manhattan distance detector reaches the threshold voltage with the specified Manhattan distance. In this figure, we can confirm that the time becomes large in proportion

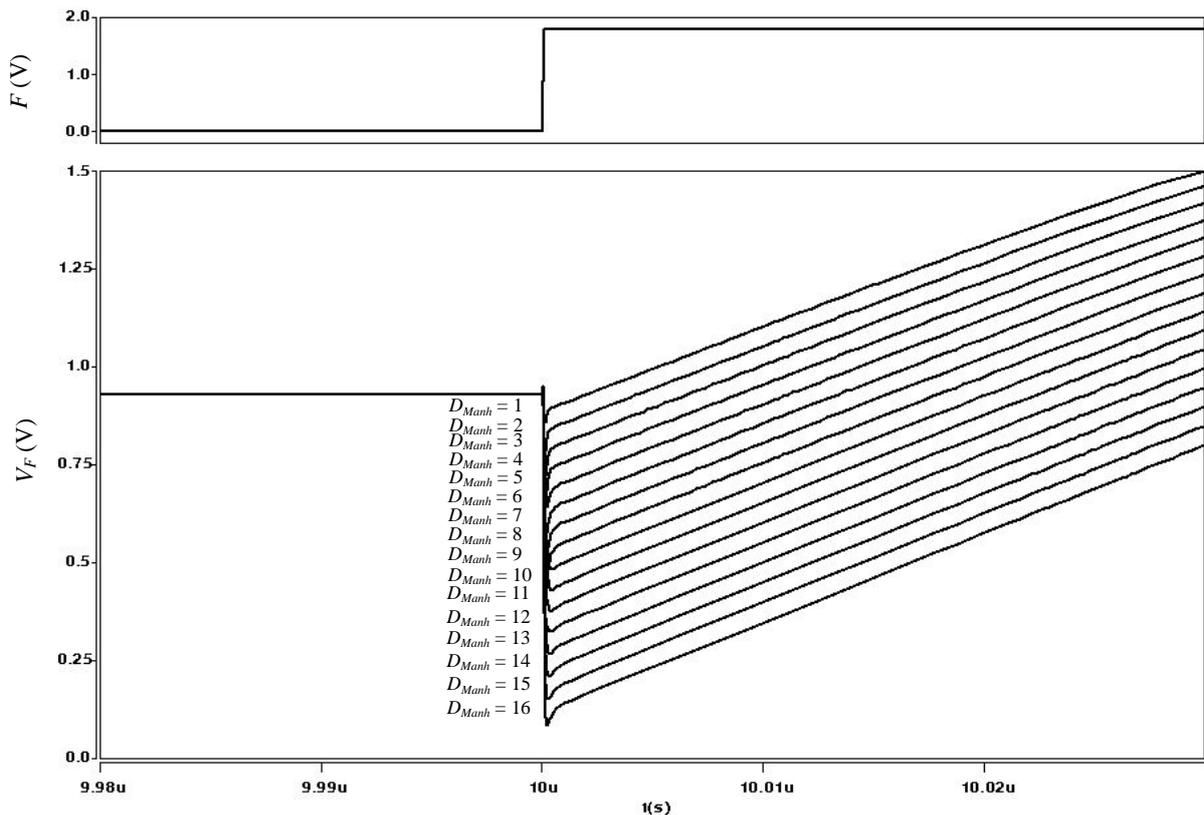


FIGURE 3. Simulated results of the floating gate voltage as a function of time

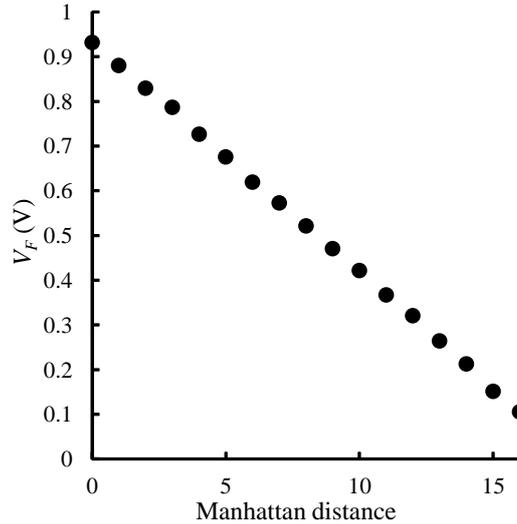


FIGURE 4. Relationship between the floating gate voltage and the Manhattan distance

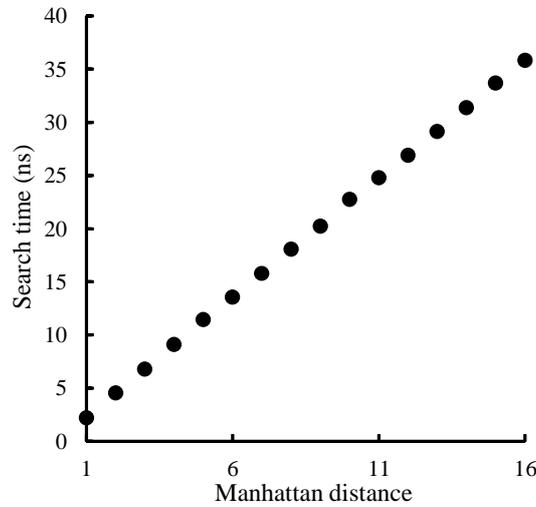


FIGURE 5. Relationship between the search time and the Manhattan distance

to the specified Manhattan distance. Also, this result satisfies (15). In these simulations, the search time is 35.8ns when SP is 16.

Table 1 shows the summary of the I/O patterns used in the simulation for confirming the searching range, where the table expresses the input data \mathbf{A} , the reference data \mathbf{B}_k , the Manhattan distance between the input data and the reference data, the range specification, and corresponding output.

Figure 6 demonstrates the simulated results under conditions of Table 1. In this simulation, the control signal SP is inputted 2 Manhattan distance, and the outputs OUT_1 , OUT_2 , and OUT_3 corresponding to the B_1 , B_2 , and B_3 within 2 distance are in a high-level. Because, when the control voltage F becomes a high level, the floating gate voltages of the Manhattan distance detector with the reference data within 2 Manhattan distance reach the threshold voltage before the floating gate voltage of the circuit for specifying the range of Manhattan distance reaches the threshold voltage and the charging is stopped. In the simulations, power consumption of the proposed circuit is 1.82mW.

TABLE 1. An example of the I/O data in HSPICE simulations

Input data	Reference data	Manhattan distance	Range specification	Output
A $(A_1 = 5,$ $A_2 = 10)$	$B_1(B_{1,1} = 6, B_{2,1} = 10)$	1	SP $(SP_1 = 2,$ $SP_2 = 0)$	OUT_1
	$B_2(B_{1,2} = 6, B_{2,2} = 10)$	2		OUT_2
	$B_3(B_{1,3} = 6, B_{2,3} = 10)$	1		OUT_3
	$B_4(B_{1,4} = 6, B_{2,4} = 10)$	3		OUT_4
	$B_5(B_{1,5} = 6, B_{2,5} = 10)$	4		OUT_5
	$B_6(B_{1,6} = 6, B_{2,6} = 10)$	5		OUT_6
	$B_7(B_{1,7} = 6, B_{2,7} = 10)$	6		OUT_7
	$B_8(B_{1,8} = 6, B_{2,8} = 10)$	7		OUT_8

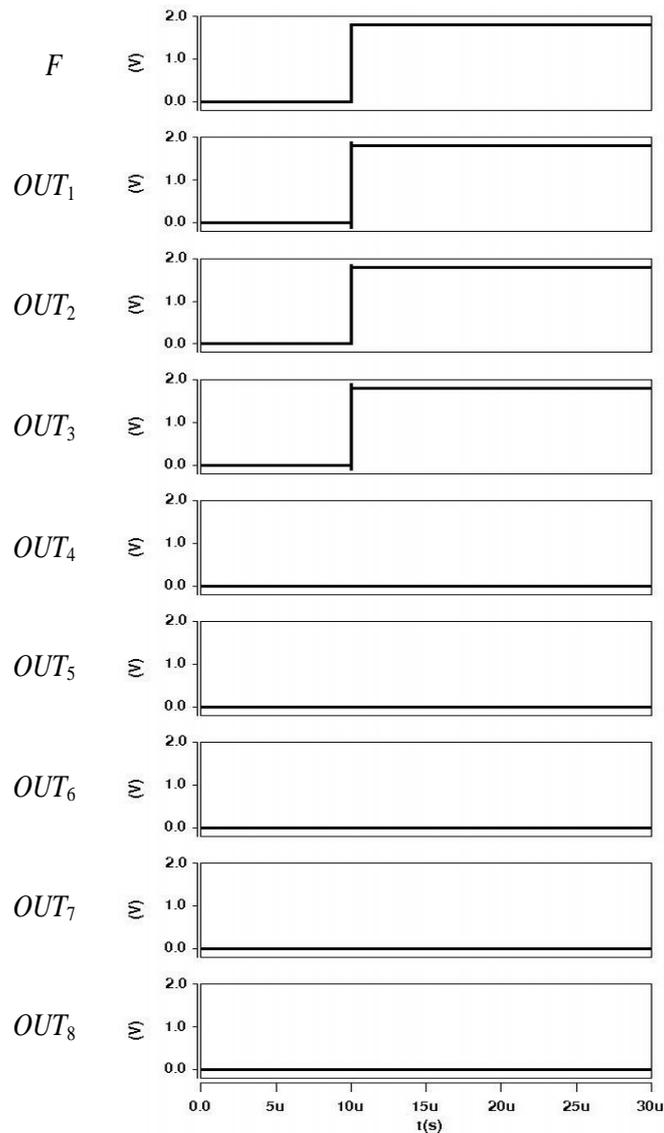


FIGURE 6. Simulated output waveforms of the proposed circuit

4. **Conclusion.** In this paper, we proposed the wide range Manhattan distance search circuit. The proposed circuit can be designed by modifying the minimum Manhattan distance search circuit. The proposed circuit retrieves all reference data within the specified

Manhattan distance. The circuit configuration of the proposed circuit is simple, because the circuit is constituted by adding only one Manhattan distance detector for specifying the range of the Manhattan distance to the minimum Manhattan distance search circuit. Furthermore, we revealed that the proposed circuit is not affected by the variation of the threshold voltage with manufacturing and temperature and the initial charge of the neuron CMOS inverters.

We were able to derive the expected results by HSPICE simulations using $0.18\mu\text{m}$ CMOS process of ROHM Semiconductor. In the simulations, the search time of the proposed circuit was 35.8ns when SP was 16 and the power consumption was 1.83mW.

In future, we are going to integrate the proposed circuit and verify the performance through the experiments of a fabricated IC chip.

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