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NOVEL OPTIMAL HARMONIC MITIGATION BASED ON MOPSO TO CONTROL SWITCHING OF ODD-NARY MULTILEVEL INVERTER

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Abstract. *Providing a high-level staircase sinusoidal voltage with reduced structures is a prominent issue in front of innovative multilevel inverters. Low total harmonic distortion (THD), low number of components and high number of output voltage levels are recognized as the salient advantages of these multilevel inverters. In this paper, a novel multilevel inverter is introduced to provide high-level staircase sinusoidal voltage with consideration of the low number of switches. The sub-multilevel inverter has been constructed by capacitor voltage dividers which are clamped with H-bridge inverter via bi-directional switches. Depending on the values of these capacitors, the suggested multilevel inverter can flexibly act in accordance with self-defined "Odd-nary" principle. In order to acquire desired fundamental component of output voltage along with low THD, "scission-style" harmonic elimination pulse width modulation (HEPWM) based on multi objective particle swarm optimization (MOPSO) is introduced to optimally trigger the switches' gates.*

Keywords: Odd-nary multilevel inverter, Optimal harmonic elimination, MOPSO, Voltage quality, Scission-style HEPWM

1. **Introduction.** Multilevel inverters have functionally operated to synthesize a staircase sinusoidal voltage through a number of DC voltage sources, that the number of voltage levels has determined the voltage quality of multilevel inverter [1,2]. The initial category of multilevel inverter has been suggested by Nabae et al. in the eighties [3]. Ever since, these inverters have been attracting more attention by scholars and industrial companies in many different levels of voltages, which some of these topologies have investigated in several literature aiming to solve the rating problem of semiconductors voltages and currents [4-8].

Apart from providing an appropriate staircase sinusoidal waveform, one of the salient advantages of these structures is their feasibility to apply them in higher voltage-levels which it is due to low values of: switching power losses (SPL), peak invers voltage (PIV) on switches, and dV/dt [9-11]. Another particular advantage of these multilevel inverters is creation of sinusoidal voltage with low harmonic component, without growing the frequency of switching or reducing the inverter output power [12-14].

Multilevel inverter is recognized as one of the state-of-the-art inverters in the field of power electronics. They have been successfully applied in many industrial applications like high voltage direct current (HVDC), flexible alternative current transmission system (FACTS), photo-voltaic (PV), uninterruptible power supplies (UPS) and industrial drive applications. Multilevel inverters are generally categorized into three class viz. cascaded H-bridge (CHB), neutral point clamped (NPC), flying capacitors (FC) [15-17]. It is

worth mentioning that, these types of inverters encompass a number of components, e.g., switches, capacitors, diodes and the same in order to create high-level staircase sinusoidal voltage. In recent years, many different inverters with special configurations have emerged to provide high-level staircase sinusoidal voltage [18-21]. Despite that, these structures have been constructed by large number of components. Hitherward, it would be practically impressive that the number of semiconductor switches to be reduced. The scientific researchers are wordwidely expending the great attempts to introduce new and upgraded multilevel inverters with reduced components so that the voltage quality and financial problems of these structures to be unraveled [22-26]. Such these reduced structures have functionally introduced with the aim of acquiring the high-level staircase sinusoidal voltage with considering the low number of switches. In this regard, a new multilevel inverter is here suggested so that the number of output voltage levels increased. The suggested sub-multilevel inverter has been constructed by the flying capacitor structure clamped to H-bridge via bi-directional switches. Depending on values of these capacitors, the suggested multilevel inverter can flexibly act in accordance with self-defined "Odd-nary" principle. The scholars have been recently attempting to enhance the voltage quality of multilevel inverters. In this regard, the produced undesirable harmonics by multilevel inverters with equal DC sources can be eliminated using the expedient modulation methods, e.g., PWM and SVPWM [27,28]. Unfortunately, these methods cannot appropriately eliminate the lower order harmonics. Another technique is based on choosing the switching angles to mitigate the lower order harmonics, e.g., the 5th, 7th, 11th, and 13th from the output voltage of inverter which is named selective harmonic elimination (SHE) [29-31]. A substantial problem related to such approaches is to acquire the arithmetic solution of nonlinear transcendental equations that involve trigonometric clauses. These nonlinear equations could be unraveled using iterative approaches such as Newton-Raphson technique [32]. This method highly depends on an appropriate initial estimation; otherwise, it might be located in local optima. Hence, this method cannot be practicable for solution of the SHE problem with a great number of switching angles while appropriate initial estimations are not available. In another approach, the transcendental equation has been converted into the polynomial equations [33,34]; next the resultant theory is employed to figure out all feasible solutions sets. While the number of voltage levels is increased, the computational burden is significantly heightened. Heuristic algorithms due to the high ability to solve the complex objective functions have been affluently employed to unravel the aforesaid drawbacks.

In this regard, in order to upgrade the ability of SHE scheme and accordingly acquire high voltage quality, i.e., desired fundamental component and low THD, the "scission-style" HEPWM based on the optimization problem has been appointed. Due to nature of multi-objective problem, the implementation of multi-objective optimization technique is not avoidable. Hence, MOPSO is here applied to unraveling the non-linear objectives. Eventually, the relevant analytical analysis accompanied by the simulation results has transparently corroborated the performance of suggested multi-level inverter. Furthermore, the improvement of voltage quality scheme using "scission-style" HEPWM strategy based on MOPSO has been well approved.

The other sections of this paper are systemized as follows. The suggested multilevel inverter has been detailed in Section 2. The suggested HEPWM based on MOPSO has been described in Section 3 toward enhancement of the voltage quality of multilevel inverter. In Section 4, non-dominated sorting MOPSO principle has been explained. In Section 5, the voltage quality of multilevel inverter based on three different scenarios has been carried out. In the end, the conclusion is presented in Section 6.

2. **Suggested Odd-nary Multilevel Inverter.** A new inverter topology is here introduced to improve the voltage quality despite low number of switches. This structure can operate in the symmetric and asymmetric conditions. As can be seen in Figure 1, substructure of the proposed multilevel inverter has been constructed by DC voltage sources, capacitors and unidirectional/bidirectional switches. Sub-multilevel inverters would be cascaded to construct the overall configuration of the proposed odd-nary multilevel inverter.

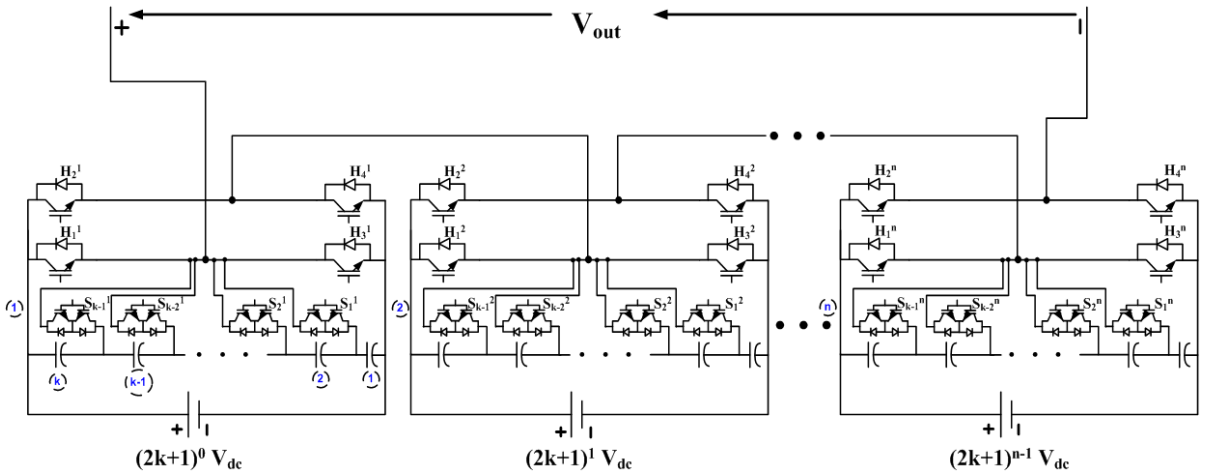


FIGURE 1. Proposed odd-nary multilevel inverter

In general, the number of components utilized in this structure can be presented as follows:

$$N_{\text{uni-directional}} = 4.N_{\text{Source}} \tag{1}$$

$$N_{\text{bi-directional}} = (k-1).N_{\text{Source}} \tag{2}$$

$$N_{\text{Switch}} = (k+3).N_{\text{Source}} \tag{3}$$

$$N_{\text{capacitor}} = k.N_{\text{Source}} \tag{4}$$

While, k, N_{Source}, $N_{\text{uni-directional}}$ and $N_{\text{bi-directional}}$ are the number of capacitors in each sub-multilevel inverter, DC voltage sources, unidirectional switches and bidirectional switches, respectively. However, values of DC voltage sources have followed from the geometric progression with different ratios so that the required sinusoidal voltage with uniform step to be earned. Behaviour of this structure as operated in both symmetric and asymmetric states has been detailed in following subsections.

2.1. **Symmetrical operation of multilevel inverter.** In accordance with the numbers of bidirectional semiconductor switches, capacitors and module along with pertinent switching manoeuvre the quasi-sinusoidal voltage with expedient levels will be created. In symmetrical operation, DC voltage sources have the similar values up to V_{dc}. The number of steps would be increased via adding bidirectional semiconductor switches and capacitors. Sub-multilevel inverter has functioned as voltage synthesizer that with considering: one bidirectional switch and two capacitors ($k = 2$) create five levels, two bidirectional switches and three capacitors ($k = 3$) create seven levels, and also in the same way $k - 1$ bidirectional switch and k capacitors create $2k + 1$ levels. The output voltage of each sub-multilevel inverter and the overall output voltage of multilevel inverter considering $k = 2$ and $n = 2$ are given in Figure 2.

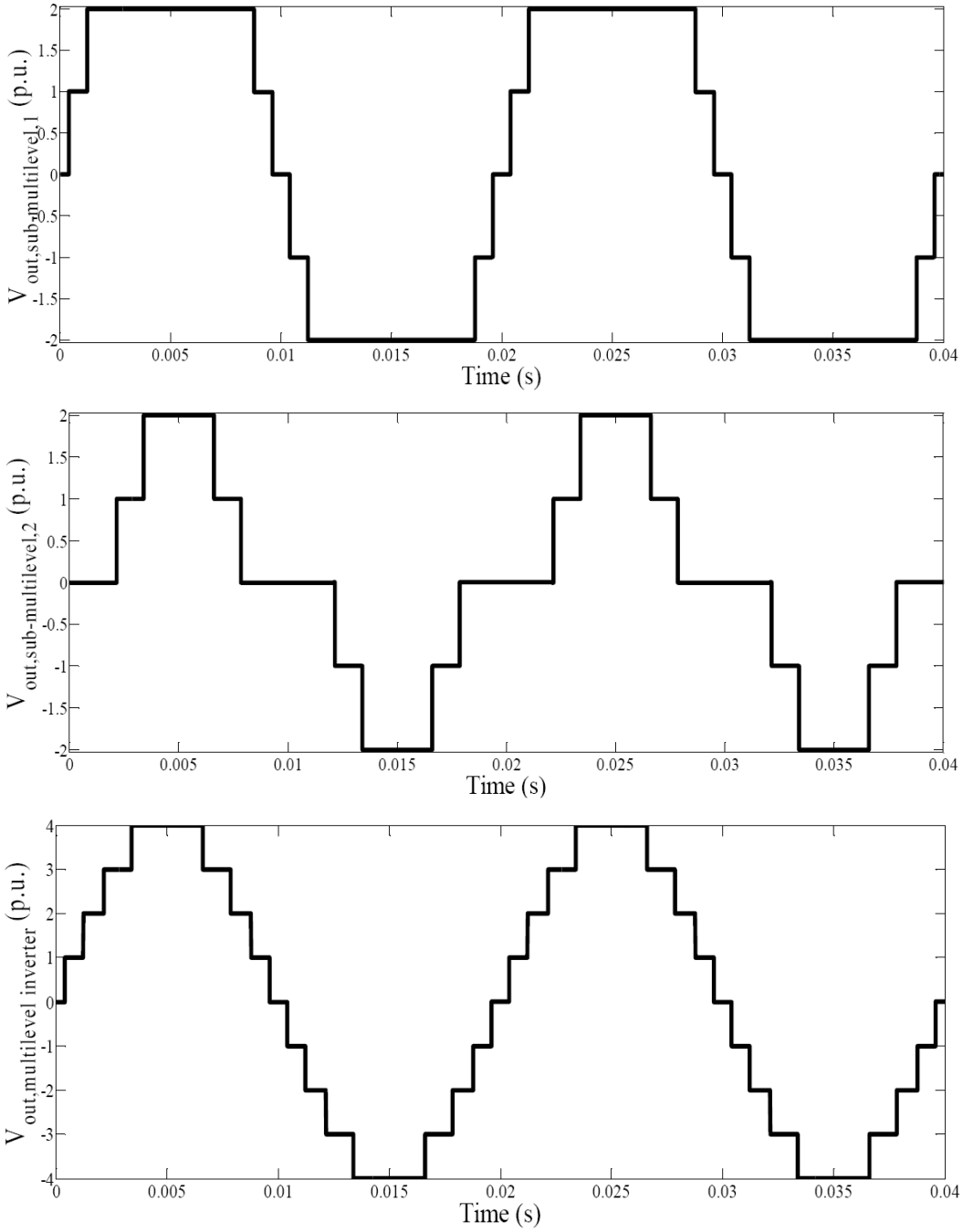


FIGURE 2. Output voltage of the proposed multilevel inverter in symmetrical status

It is presumed that each sub-multilevel inverter has k capacitors, and all capacitors have equal values. Then the input value of each sub-multilevel inverter in terms of capacitors value can be given by:

$$V_{\text{in, sub-multlvel}} = \sum_{j=1}^{k} V_{c,j} \tag{5}$$

where $V_{c,1} = V_{c,2} = \cdots = V_{c,k} = V_c$. Thus,

$$V_{\text{in, sub-multlvel}} = k.V_c = V_{dc} \tag{6}$$

By summing the output voltage of sub-multilevel inverter, the maximum output voltage created by the proposed multilevel inverter can be presented by:

$$V_{o,\,\max,\,\text{symmetric}} = \sum_{i=1}^{n} V_{\text{in,\,sub-multlvel},i} = N_{\text{Source}}.k.V_c = N_{\text{Source}}.V_{dc} \tag{7}$$

Also, the number of output voltage levels will be:

$$M_{\text{Level,\,symmetric}} = 2.\left(k.V_{o,\,\max,\,\text{symmetric}}\right)/V_{dc} + 1 \tag{8}$$

2.2. **Asymmetrical operation of multilevel inverter.** To create staircase sinusoidal voltage with high level number with no addition of any components, the suggested multilevel inverter has operated in asymmetrical status. In this condition, the values of DC voltage sources are not equal which have been increased according to the special geometric progression. Assumed that each sub-multilevel inverter has k capacitors, accordingly the values of DC voltage sources in terms of capacitors' values for the first sub-multilevel inverter can be presented by:

$$V_{\text{in,\,sub-multlvel,\,1}} = \sum_{j=1}^{k} V_{c,j} \tag{9}$$

where $V_{c,1} = V_{c,2} = \cdots = V_{c,k} = V_{c1}$. Thus,

$$V_{\text{in,\,sub-multlvel}} = k.V_{c1} = V_{dc} \tag{10}$$

Then, the values of DC voltage sources in each sub-multilevel inverter can be defined by:

$$V_{\text{in,\,sub-multlvel},i} = [2j+1]^{i-1} V_{dc} \tag{11}$$

where $j = 2, 3, \ldots, k$ and $i = 1, 2, \ldots, n$.

By summing the output voltage of sub-multilevel inverter, the maximum output voltage created by odd-nary multilevel inverter can be given by:

$$\begin{aligned} V_{o,\,\max,\,\text{asymmetric}} &= \sum_{i=1}^{n} V_{\text{in,\,sub-multlvel},\,i} \\ &= \frac{\left((2k+1)^{N_{\text{Source}}} - 1\right)}{2} k.V_{c1} \\ &= \frac{\left((2k+1)^{N_{\text{Source}}} - 1\right)}{2} V_{dc} \end{aligned} \tag{12}$$

Also, the number of output voltage levels will be:

$$M_{\text{Level,\,asymmetric}} = \left(2V_{o,\,\max,\,\text{asymmetric}}\right)/V_{dc} + 1 \tag{13}$$

The strongpoint of the suggested multilevel inverter is its high flexibility to operate in the statuses of: "Quinary" with considering one bidirectional switch and two capacitors ($k = 2$), "Septenary" with considering two bidirectional switches and three capacitors ($k = 3$), "Nonary" with considering three bidirectional switches and four capacitors ($k = 4$), "Undenary" with considering four bidirectional switches and five capacitors ($k = 5$), and also in the same way the suggested odd-nary multilevel inverter has been earned. The output voltage of each sub-multilevel inverter and the overall output voltage of odd-nary multilevel inverter considering $k = 2$ and $n = 2$ are presented in Figure 3.

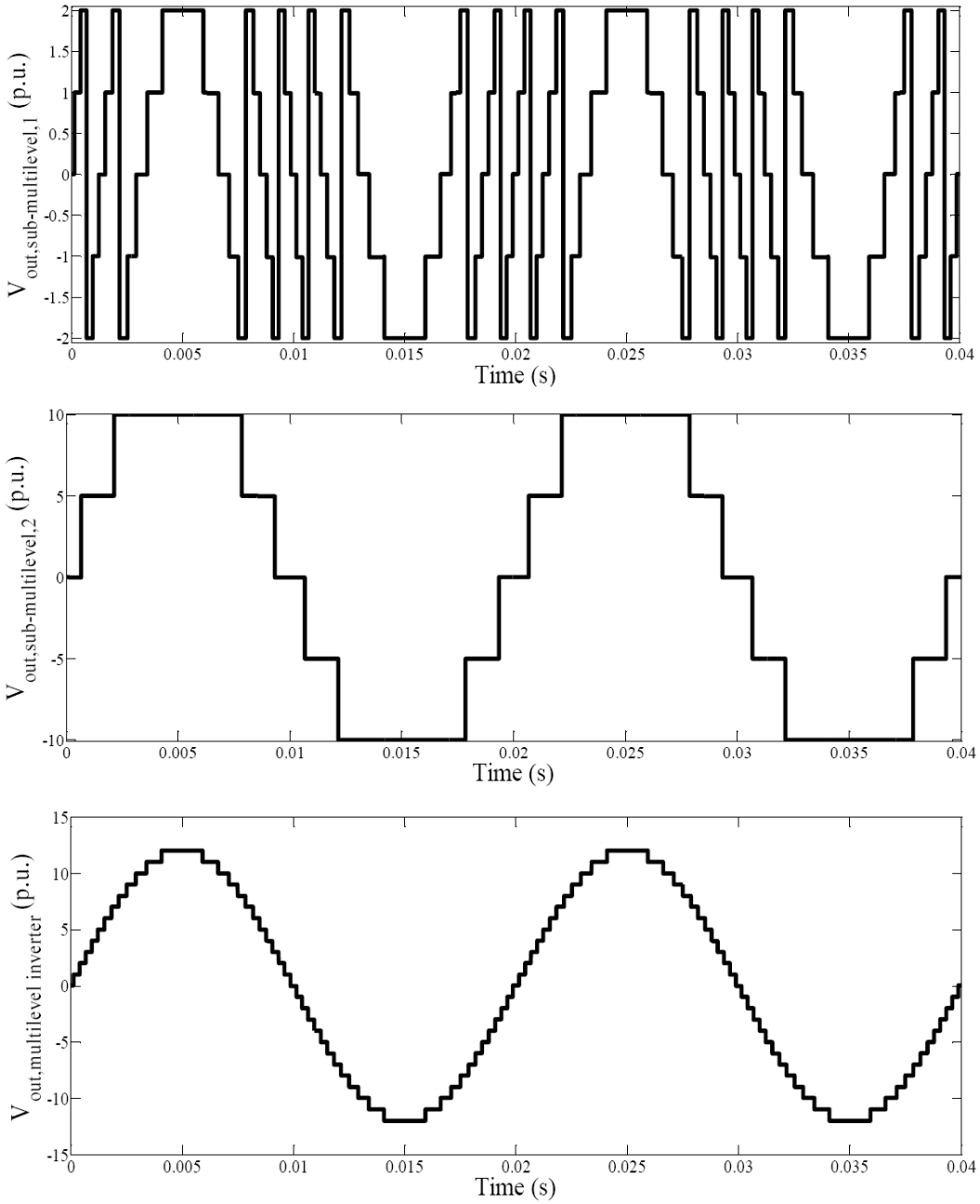


FIGURE 3. Output voltage of the proposed multilevel inverter in asymmetrical status

2.3. **Comparison of suggested multilevel inverter with others.** The performance of suggested structure has been compared with other available structures in viewpoint of the number of output voltage levels versus the number of utilized switches. To do accurate comparison, the suggested multilevel inverter in symmetrical/asymmetrical condition has been compared with other innovative and popular symmetrical/asymmetrical multilevel inverters. In order to portray the performance of the suggested multilevel inverter, some popular and recently introduced symmetrical and asymmetrical multilevel inverters have been dealt with.

Symmetrical multilevel cascaded inverters: The relationships between the numbers of utilized switches in these structures: CHB, [35-38] in terms of the numbers of their created

voltage levels can be respectively presented by:

$$N_{\text{Switch, [CHB]}} = 2(\text{M}_{\text{Level}} - 1) \tag{14}$$

$$N_{\text{Switch, [35]}} = (\text{M}_{\text{Level}} + 1) \tag{15}$$

$$N_{\text{Switch, [36]}} = (\text{M}_{\text{Level}} + 3) \tag{16}$$

$$N_{\text{Switch, [37]}} = 3/2(\text{M}_{\text{Level}} - 1) \tag{17}$$

$$N_{\text{Switch, [38]}} = (\text{M}_{\text{Level}} + 1) \tag{18}$$

Asymmetrical multilevel cascaded inverters: the relationships between the numbers of utilized switches in these structures: Binary, Trinary, [37-40] in terms of the numbers of their created voltage levels can be respectively presented by:

$$N_{\text{Switch, Binary}} = 4\frac{\text{Ln}(\text{M}_{\text{Level}} + 1)}{\text{Ln2}} - 4 \tag{19}$$

$$N_{\text{Switch, Trinary}} = 4\frac{\text{Ln}(\text{M}_{\text{Level}})}{\text{Ln3}} \tag{20}$$

$$N_{\text{Switch, [37]}} = 6\frac{\text{Ln}(\text{M}_{\text{Level}})}{\text{Ln5}} \tag{21}$$

$$N_{\text{Switch, [38]}} = 2/3\,(\text{M}_{\text{Level}} + 5) \tag{22}$$

$$N_{\text{Switch, [39]}} = 2\frac{\text{Ln}(\text{M}_{\text{Level}} + 1)}{\text{Ln2}} + 2 \tag{23}$$

$$N_{\text{Switch, [40]}} = \left[\text{Ln}\left(\frac{\text{M}_{\text{Level}} + 1}{2}\right) \times \frac{3n - 1}{\text{Ln}(n + 1)}\right] + 4 \tag{24}$$

The curves of created levels related to popular and innovative multilevel inverters along with suggested multilevel inverter as operated in symmetrical and asymmetrical conditions have been respectively presented in Figure 4(a) and Figure 4(b).

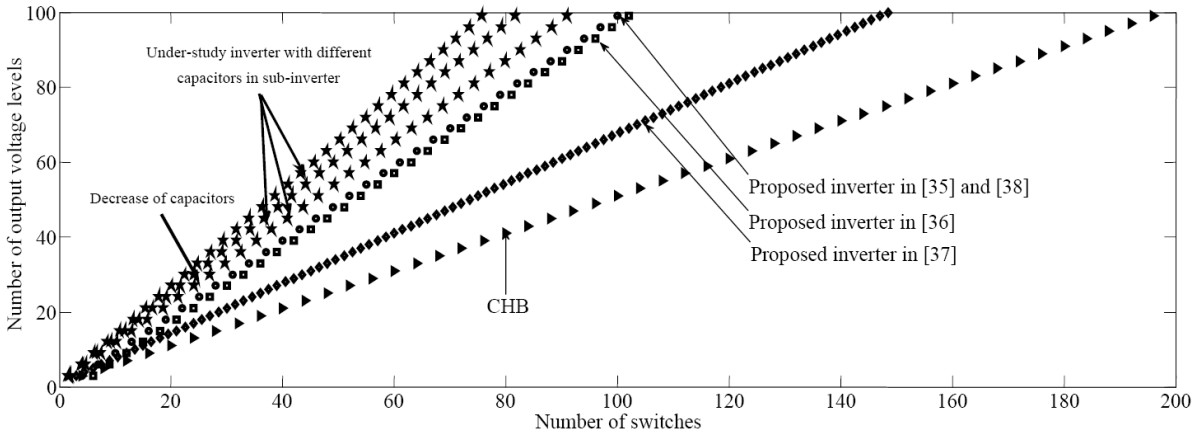
The presented curves in Figure 4(a) and Figure 4(b) have transparently confirmed the high performance of suggested cascaded multilevel inverter to provide staircase sinusoidal voltage waveform with high levels number against the low number of switches as compared to others. It means that, the prominent issues in designing multilevel inverters, i.e., voltage quality, low THD, structure's cost price are acquired.

3. **Voltage Quality Enhancement Based HEPWM.**

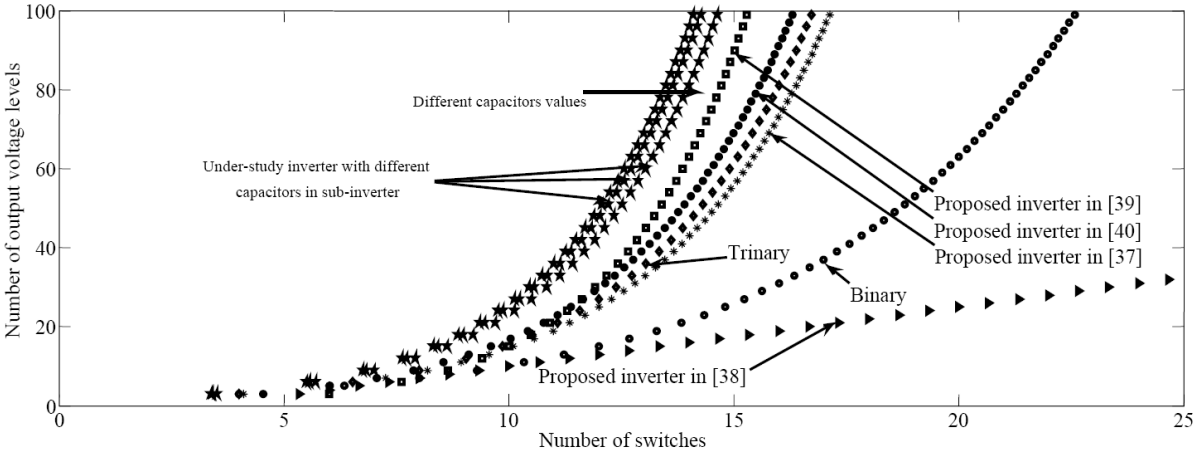
3.1. **Harmonic elimination principle.** Provided the number of inverter's components to be increased, the voltage quality problem becomes paler. From both technological and economical standpoints, voltage quality of the suggested cascaded multilevel inverter has been enhanced with considering ten switches so that two prominent issues: desired fundamental of output voltage and low value of THD to be obtained. Since then, nine levels symmetric status of the suggested structure has been taken into account to better demonstrate the harmonic elimination problem. The staircase sinusoidal voltage waveform can be fundamentally expanded in Fourier series which is expressed as follows:

$$\upsilon_{out}(\alpha) = A_0 + \sum_{n=1}^{\infty} A_n.\cos(n\alpha) + B_n.\sin(n\alpha) \tag{25}$$

$$\begin{cases} A_0 = (2\pi)^{-1}\int_0^{2\pi} V_{out}(\alpha).d\alpha \\ A_n = (\pi)^{-1}\int_0^{2\pi} V_{out}(\alpha).\cos(n\alpha).d(\alpha) \\ B_n = (\pi)^{-1}\int_0^{2\pi} V_{out}(\alpha).\sin(n\alpha).d\alpha \end{cases} \tag{26}$$



(a)



(b)

FIGURE 4. (a) Number of created levels versus number of switches as operated symmetrical status; (b) number of created levels versus number of switches as operated asymmetrical status

Forasmuch as the average value or DC component of the output voltage created by multilevel inverter is not available $A_0 = 0$. In accordance with the general staircase sinusoidal waveform of multilevel inverter presented in Figure 5(a), being odd function withal quarter-wave symmetry, only sinusoidal part of Fourier series with presence of odd harmonics would appear, i.e.,

$$\upsilon_{out}(\alpha) = \sum_{n=1,3,5,\ldots}^{\infty} B_n . \sin(n\alpha) \tag{27}$$

3.2. **HEPWM triggering strategy.** HEPWM has been functionally set assigned to eliminate undesirable harmonics from the staircase sinusoidal waveform created by PWM technique. Conventional HEPWM method has some prominent disadvantages. The first, a number of semiconductors, DC voltage sources and the suchlike are required to create high-level staircase sinusoidal voltage for mitigation of all the harmonics while this trend is not cost-effective. The second, since the suggested symmetric inverter module has been triggered just twice in each quarter cycle, the perfect performance of these switches has not been used. Toward this subject, the "scission-style" HEPWM that can modulate a number of angles within specific level provides staircase sinusoidal voltage waveform with

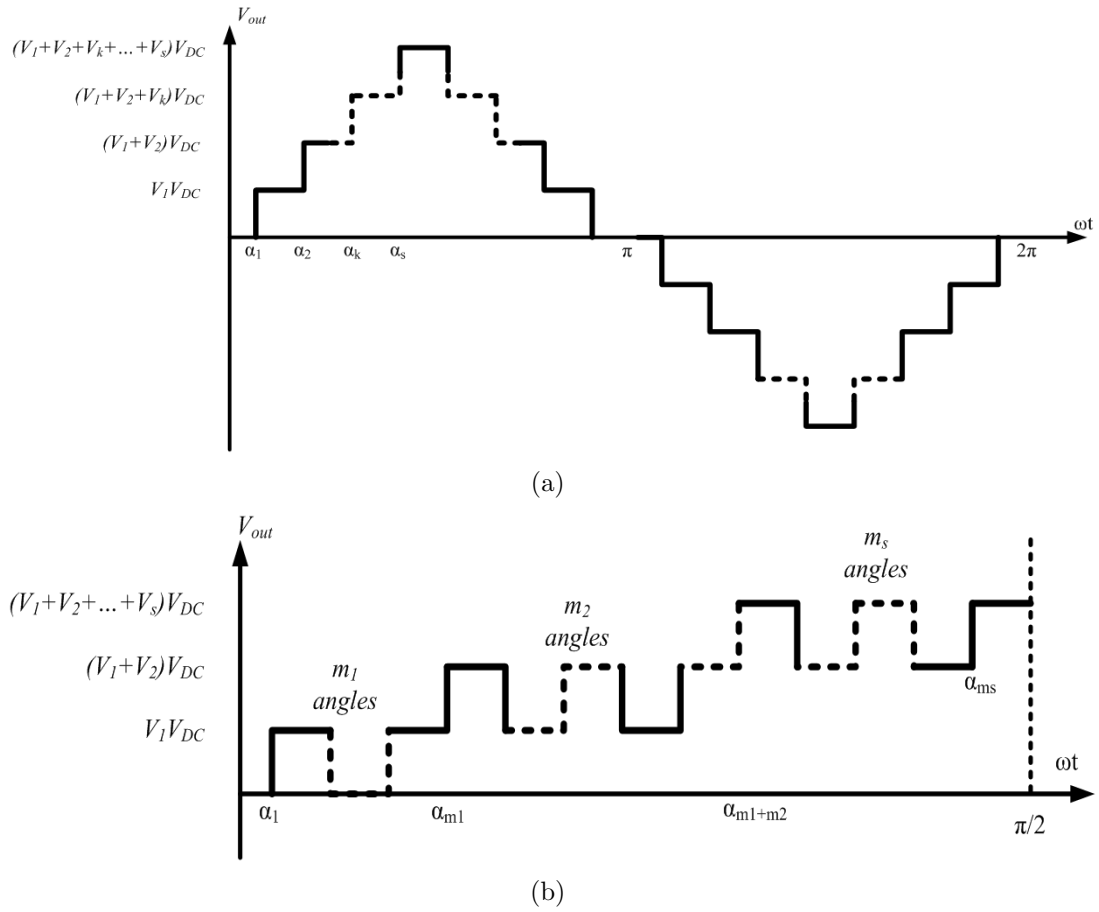


FIGURE 5. (a) General staircase sinusoidal waveform of multilevel inverter; (b) scission-style HEPWM quarter cycle waveform of multilevel inverter

several scissions in each level as shown in Figure 5(a). The most prominent feature of "scission-style" HEPWM is its high ability to eliminate further harmonics despite low levels, i.e., low number of switches and DC voltage sources. Furthermore, utilization of unequal DC power supplies can more augment the effectiveness of this approach to more mitigate harmonic components. However, the problem formulation is scheduled with different values of: DC voltage sources, pulses width and triggering angles which can be perceived with envisaging Figure 5(b).

Fourier series expansion of the stepped output voltage waveform of the multilevel inverter can be expressed by Equation (28):

$$\upsilon_{out}(\omega t) = \sum_{n=1,3,5,\ldots}^{s} \left\langle \frac{4V_f}{n\pi} \cdot \left[\upsilon_1 \sum_{i=1}^{m_1} (-1)^{i+1} \cos n\alpha_i \pm \upsilon_2 \sum_{i=m_1+1}^{m_2} (-1)^{i+1} \cos n\alpha_i \right. \right. \\ \left. \left. \pm \ldots \pm \upsilon_s \sum_{i=m_{(s-1)}+1}^{m_s} (-1)^{i+1} \cos n\alpha_i \right] \right\rangle \sin(n\omega t) \tag{28}$$

where s is the number of DC voltage sources, and the created V_kV_{DC} is the value of the kth DC voltage source. $V_1 = V_2 = \cdots = V_s = 1$ while all DC voltage sources have equal values. Also, $\alpha_1 \cdots \alpha_{m_1}$ are the triggering transitions in the first level, $\alpha_{m_1+1} \cdots \alpha_{m_1+m_2}$ are the triggering transitions in the second level, and so $\alpha_{m_1+m_2+\cdots+1} + \cdots + \alpha_{m_1+m_2+\cdots+m_s}$ are the triggering transitions in the latest level.

The solution set will be attained using maintaining the value of fundamental component of output voltage in desirable value, V_f, and all the harmonics except first set to be zero as for Equations (29)-(31).

$$\hbar_1 = \left[\sum_{i=1}^{m_1} (-1)^{i-1} \cos\alpha_i + \sum_{i=m_1+1}^{m_2} (-1)^{i-(m_1+1)} \cos\alpha_i + \cdots + \sum_{i=m_{(s-1)}+1}^{m_s} (-1)^{i-\left(m_{(s-1)}+1\right)} \cos\alpha_i \right] = M \tag{29}$$

$$\hbar_2 = \left[\sum_{i=1}^{m_1} (-1)^{i-1} \cos 5\alpha_i + \sum_{i=m_1+1}^{m_2} (-1)^{i-(m_1+1)} \cos 5\alpha_i + \cdots + \sum_{i=m_{(s-1)}+1}^{m_s} (-1)^{i-\left(m_{(s-1)}+1\right)} \cos 5\alpha_i \right] \tag{30}$$

$$\hbar_m = \left[\sum_{i=1}^{m_1} (-1)^{i-1} \cos(3m-2)\alpha_i + \sum_{i=m_1+1}^{m_2} (-1)^{i-(m_1+1)} \cos(3m-2)\alpha_i + \cdots + \sum_{i=m_{(s-1)}+1}^{m_s} (-1)^{i-\left(m_{(s-1)}+1\right)} \cos(3m-2)\alpha_i \right] \tag{31}$$

Also, the modulation index can be determined by Equation (32) and Equation (33):

$$M = \frac{\pi V_f}{4V_{DC}}, \quad 0 \le M \le S \tag{32}$$

$$M_i = M/S, \quad 0 \le M_i \le 1 \tag{33}$$

3.3. **Objective function.** The optimal problem based on MOPSO has been solved by minimizing Equation (34) and Equation (35) which will be explained in the next section.

$$F_1 = THD = V_f^{-1} \cdot \sqrt{\sum_{i=2}^{\infty} \hbar_i^2} \tag{34}$$

$$F_2 = |\hbar_1 - M| \tag{35}$$

An accurate sequencing of the triggering angles based on HEPWM has been defined to provide relevant scission points in each level, i.e.,

$$0 \le \alpha_1 < \alpha_2 < \cdots < \alpha_{m_1} < \cdots < \alpha_{m_s} \le \pi/2 \tag{36}$$

The suggested approach is also assigned based on non-equal DC voltage sources concept. Thus, the problem constraints related to this non-equality is presented as follows:

$$0 < V_1 \ne V_2 \ne \cdots \ne V_s \le 1 \tag{37}$$

Furthermore, the multilevel inverter can generate quasi-sinusoidal waveform with different pulse-widths that can highly enhance the performance of "scission-style" HEPWM approach. Hence, the relevant limitation can be given by:

$$0 < \alpha_{m_1} < \alpha_{m_2} < \cdots < \alpha_{m_s} < \pi/2 \tag{38}$$

The optimization problem is constructed into the specific search space with considering the aforementioned constraints.

4. Multi-Objective Particle Swarm Optimization.

4.1. **MOPSO overview.** PSO, one of the distinguished swarm intelligent approaches, has been stimulated from the gregarious behavior of fish and birds within the herd. Every swarm's particle adjusts its relevant course with respect to its own flight experience along with other flying experience of the particles within its contrast in the search space [41].

4.2. **Fundamental conceptions of multi objective approach.** The problem solution is mathematically introduced by [42]:

Figure out X that optimizes:

$$f(X) = [f_1(X), f_2(X), \ldots, f_k(X)] \tag{39}$$

Subject to:

$$g_i(x) \leq 0; \quad i = 1, 2, \ldots, n \tag{40}$$

$$h_j(x) \leq 0; \quad j = 1, 2, \ldots, p \tag{41}$$

where $X = [X_1, X_2, \ldots, X_n]$ is decision variables' vector, f_i, $i = 1, 2, \ldots, k$ indicate the cost functions and g_i, h_i, $i = 1, 2, \ldots, m$, $j = 1, 2, \ldots, p$ indicate the problem's limitations.

The optimization problems based on multi-objective have been actually constructed in order to figure out an appropriate trade-off. For more perception of the Pareto approach, some definitions are presented as follows.

Definition 4.1. *Crate two vectors X, $Y \in R^n$, is referred to $X \leq Y$ if $x_i \leq y_i$ for $i = 1, 2, \ldots, k$, and that X dominates Y (pointed to by $X < Y$) if $X \leq Y$ and $X \neq Y$.*

Definition 4.2. *Expressed that a vector of resolution variables $X \in x \subset R^n$ is non-dominated according to x, provided no $X' \in x$ to the extent that $f(X') < f(X)$.*

Definition 4.3. *Expressed that a vector of resolution variables $X^* \in F \subset R^n$ (F indicates expedient area) is Pareto optimal provided to be non-dominated according to F.*

Definition 4.4. *Pareto optimal set P^* is defined by:*

$$P^* = \{X \in F | X \text{ is Pareto optimal}\} \tag{42}$$

Definition 4.5. *Pareto front PF^* is defined as follows:*

$$PF^* = \left\{f(X) \in \mathcal{R}^k | X \in P^*\right\} \tag{43}$$

4.3. **Mechanism of particle swarm optimization.** Both the velocity and location related to the particles can be mathematically presented by:

$$v_{i,d}^{(t+1)} = \psi \left[w \times v_{i,d}^{(t)} + c_1 + r_1 \times \left(pbest_{i,d} - x_{i,d}^{(t)}\right) + c_2 + r_2 \times \left(gbest_d - x_{i,d}^{(t)}\right)\right] \tag{44}$$

$$x_{i,d}^{(t+1)} = x_{i,d}^{(t)} + v_{i,d}^{(t+1)}, \quad \text{with } i = 1, 2, \ldots, n \text{ and } d = 1, 2, \ldots, m \tag{45}$$

$$v_d^{\min} \leq v_{i,d}^{(t)} \leq v_d^{\max} \tag{46}$$

$$\psi = \frac{2}{2 - \varphi - \sqrt{\varphi^2 - 4\varphi}} \tag{47}$$

$$\varphi = \varphi_1 + \varphi_2 \quad \text{where } \varphi > 4 \tag{48}$$

$$w = w_{\max} - \frac{w_{\max} - w_{\min}}{iter_{\max}} \times iter \tag{49}$$

4.4. **Principle of non-dominated sorting related to particle swarm optimization.** MOPSO occupies a supplementary cache for saving the figured out solutions as well as the search procedure. Also, it is considered the neighbour to be available in the swarm. The swarm is saved into supplementary cache in all generations following the up-to-date particles' location. Every time that maximum limit constrained on cache's size is attained, the algorithm performs non-dominated sorting to conserve the solutions position into the earliest five-fronts, presented in Figure 6.

To elicit the particles in following front, the earliest solutions of the front are temporarily neglected, and accordingly the aforementioned process is carried out again so that five fronts are figured out (Figure 6a). Every time the front is conserved into cache, it is subsequently larger than allowable limit and a crowding length is computed in order

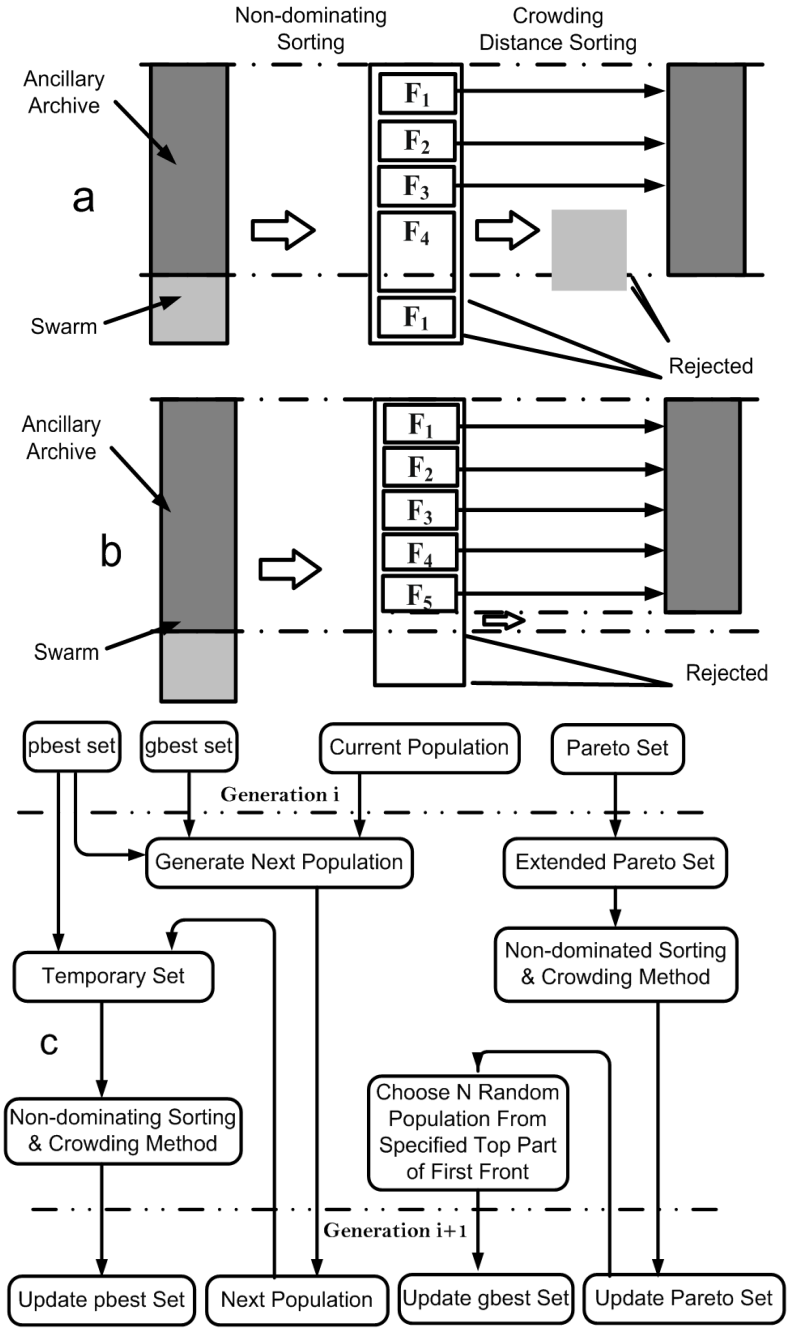
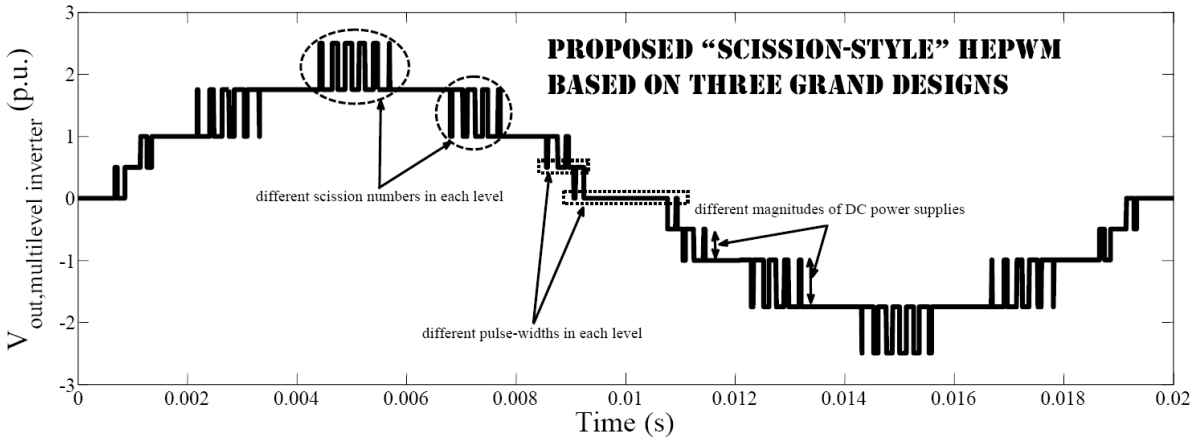


FIGURE 6. Process of non-dominated related to MOPSO method

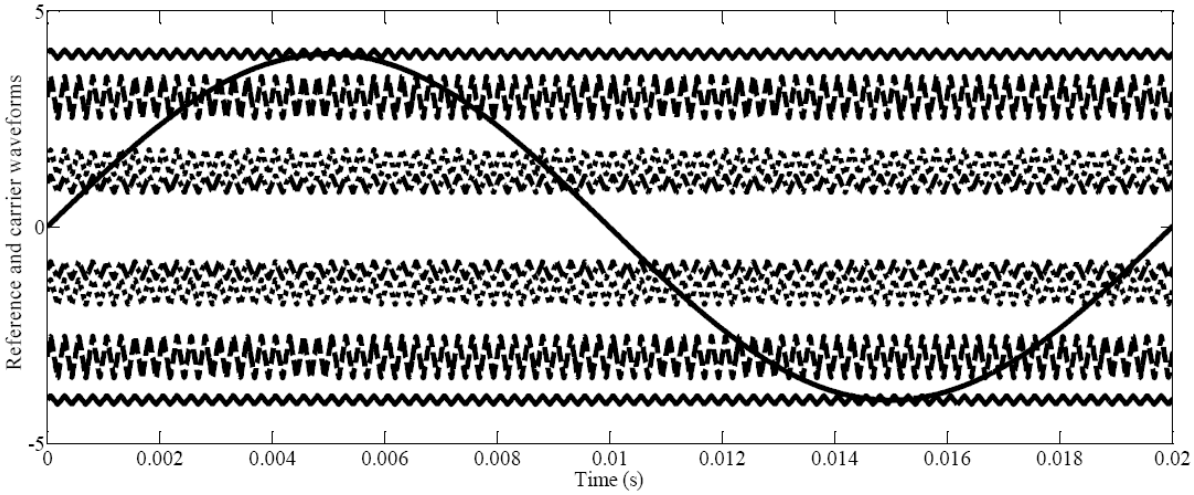
to sieve the solutions, and then next fronts are discarded (Figure 6b). Meanwhile, the flowchart of MOPSO can be presented by Figure 6c.

5. **Results and Discussion.** Scission-style HEPWM is scheduled to improve the quality voltage of the Odd-nary inverter, i.e., desired fundamental component of output voltage along with low THD. MOPSO is employed to minimize both the mentioned targets, i.e., Equation (34) and Equation (35). The flexibility of scission-style HEPWM has been set with respect to three salient criterions to more improve the voltage quality of inverter. The staircase sinusoidal voltage waveform and reference-carriers waveforms that are created according to the scission-style HEPWM are respectively portrayed in Figures 7(a) and 7(b).

5.1. **Scission-style HEPWM with respect to different scissions in each level.** As for Equation (36), the search space of MOPSO technique is constricted to a special area, and also the angles should be appropriately situated among the levels. According to Figure 5(b), m_1, m_2 and m_s represent the number of angles which are available in the first, the second and the latest levels, respectively. The angle propagation proportion is introduced as triggering angles to horn in the number of certain set angles in each level

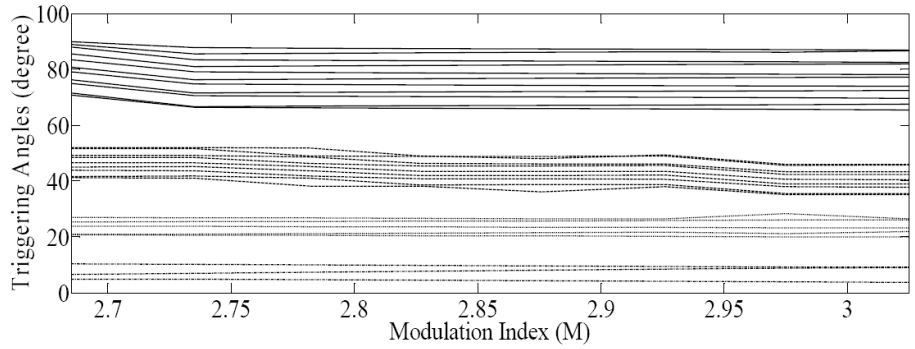


(a)

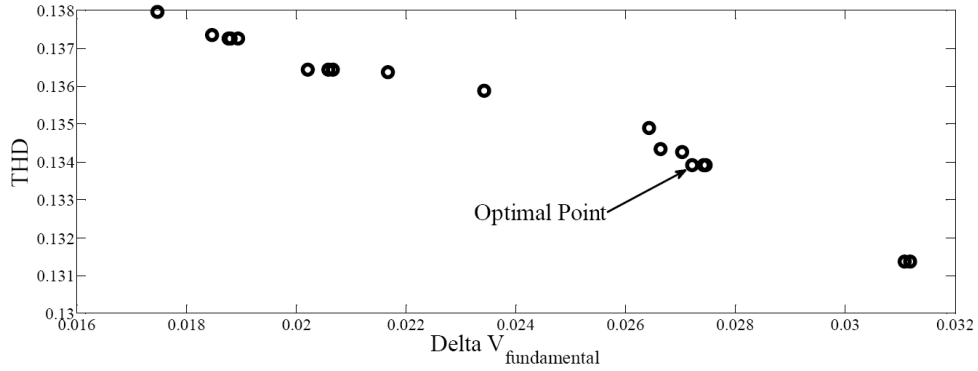


(b)

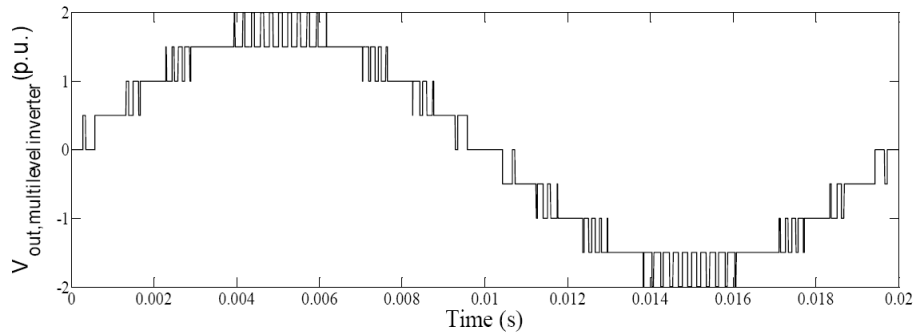
FIGURE 7. (a) Scission-style HEPWM based on three different scenarios; (b) reference and carrier waveforms based on scission-style HEPWM



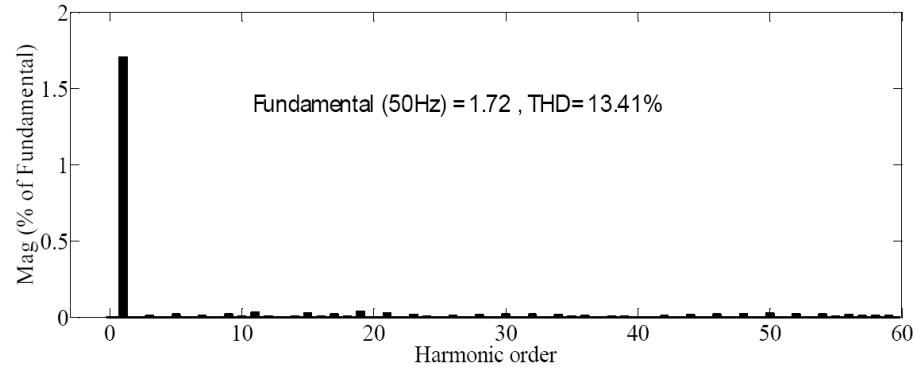
(a)



(b)



(c)



(d)

FIGURE 8. (a) Triggering angle trajectories versus values modulation index; (b) Pareto solution front of the optimization problem; (c) staircase sinusoidal voltage optimized by scission-style HEPWM-MOPSO; (d) corresponding FFT of staircase sinusoidal voltage

of output inverter voltage. This proportion is indicated by $m_1/m_2/\ldots/m_s$; e.g., for angle propagation proportion of 6/4/7/5, it has respectively indicated that first, second, third and fourth levels encompass 6, 4, 7 and 5 angles. The number of scissions in each level acts as critical function to define the value of THD, and also increase of scissions numbers in each level has decreased the value of fundamental component. Thus, the maintenance of fundamental component is one of the prominent issues for scission-style HEPWM. In this regard, MOPSO is applied to obtaining both the desired fundamental component of output voltage and low amount of THD. The optimization problem has unravelled twenty four angles in each quarter cycle of staircase sinusoidal waveform of proposed multilevel inverter. Also, the propagation proportion is taken to be 3/5/9/11 along with the modulation index ($2.68 < M < 3.03$). After finishing the optimization processes, the trajectory curve of twenty eight triggering angle and the Pareto solution front of the optimization problem are respectively given in Figures 8(a) and 8(b). Furthermore, the output voltage of suggested inverter and the relevant harmonic spectrum as to the optimum solution are respectively shown in Figure 8(c) and Figure 8(d). Here, the performance of scission-style HEPWM aimed at mitigation of the THD and maintenance of fundamental component ($1.7^{\text{p.u.}}$) is transparently conspicuous.

5.2. **Scission-style HEPWM with respect to non-equal DC voltage sources.** As for Equation (37), the constraint of non-equality of DC voltage sources is assigned. MOPSO has optimized the magnitude of DC voltage sources to minimize both Equation (34) and Equation (35). Apart from the effectiveness of triggering angle aimed at reduction

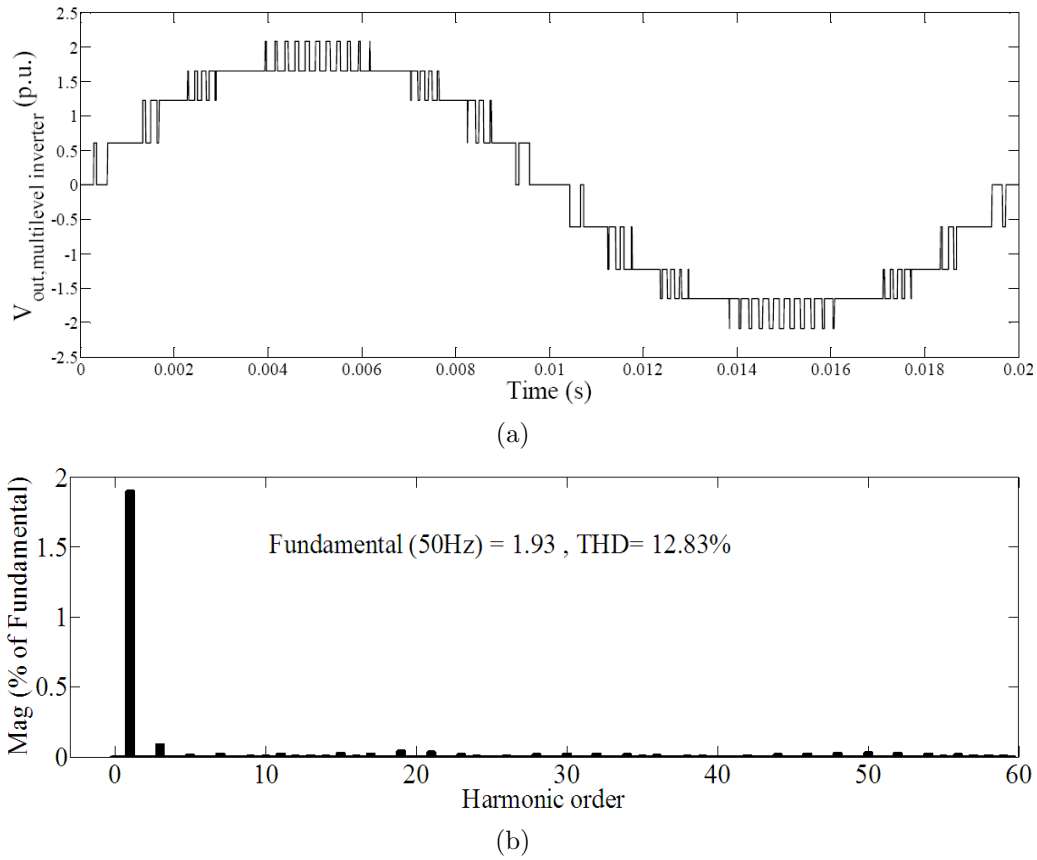


FIGURE 9. (a) Staircase sinusoidal voltage optimized by scission-style HEPWM-MOPSO; (b) corresponding FFT of staircase sinusoidal voltage

of enquired harmonic component, variety of the DC voltage sources can play an important role in this regard. After completion of optimization process, the output voltage and its harmonic spectrum are respectively presented in Figure 9(a) and Figure 9(b). These figures have clearly shown that THD is reduced by optimizing magnitude of DC voltage sources and also holding on magnitude of fundamental component in $1.9^{\text{p.u.}}$.

5.3. **Scission-style HEPWM with respect to different pulse-widths in each level.** Width of all pulses of staircase sinusoidal waveform is optimized by MOPSO so that both Equation (34) and Equation (35) to be minimized. Effectiveness of this variation in the form of output voltage of inverter along with harmonic spectrum is evident in Figure 10(a) and Figure 10(b). It is here considered that the magnitude of fundamental component is $1.8^{\text{p.u.}}$.

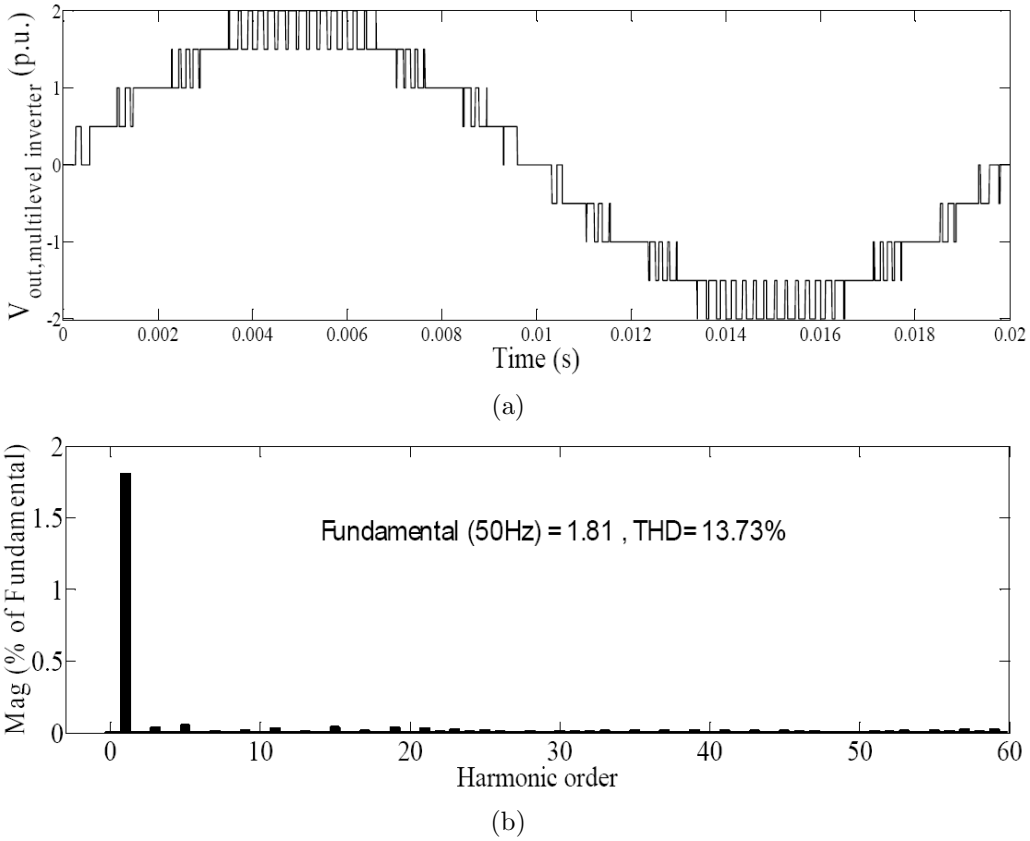


FIGURE 10. (a) Staircase sinusoidal voltage optimized by scission-style HEPWM-MOPSO; (b) corresponding FFT of staircase sinusoidal voltage

6. **Conclusion.** In this paper, a novel cascaded multilevel inverter is suggested to provide a high level staircase sinusoidal voltage with the fewest harmonics with consideration of the low number of components. To evaluate the performance of Odd-nary multilevel inverter, it has been perfectly compared with the popular and innovative symmetrical and asymmetrical multilevel inverters. Meanwhile, the voltage quality criteria, i.e., desired fundamental component of output voltage and low amount of THD has been fulfilled by self-defined scission-style HEPWM. This approach has been operated based on three distinct scenarios: different scissions, different pulse-widths and non-equal DC voltage sources. Also, due to the multi-objective nature of understudy problem and considering the high performance of MOPSO to unravel the non-linear objectives, it has been used

to solve the optimization problem. While all the relevant analytical analysis and the simulation results have been carried out, the results have clearly corroborated the performance of Odd-nary multilevel inverter and also improvement of voltage quality using scission-style HEPWM based on MOPSO.

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