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ANALYSIS OF MACROCYCLE SCHEDULES FOR AN ALTERNATIVE OF FF-BASED FEEDFORWARD CONTROL

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Abstract. *This paper focuses on analyzing the macrocycle schedules generated for an alternative implementation of Foundation Fieldbus (FF)-based feedforward control with hybrid architecture. The interested alternative control strategy is based on the use of the bias/gain (BG) function block to create feedforward summing function outside a proportional-integral-derivative (PID) function block for use to meet special operation requirements. An FF temperature control loop connected to the DeltaV distributed control system (DCS) providing built-in capability to execute function blocks in an H1 interface card is utilized as a case study to examine the effects of eight different configuration schemes on macrocycle schedules and function block synchronizations. Experimental results obtained from major configuration schemes by placing the PID block in the DCS host controller, the H1 interface card, and the temperature transmitter show that function block allocation affects the control performance to anticipate process disturbance effects.*
Keywords: Foundation Fieldbus, Feedforward, Function block, Bias/gain, Hybrid architecture, Macrocycle, Synchronization, Network load

1. **Introduction.** With the advent of digital control systems and fieldbus networks, both basic and advanced regulatory control strategies can be implemented by configuring software function blocks that consist of parameters for measurement, calculation, and control functions. A unique characteristic of function blocks established by Foundation Fieldbus (FF) technology is that they can be linked to each other for building control strategies [1]. Based on function block links, the measurement, calculation, and control can be defined independently of whether the associated function blocks are located to perform in FF H1 field devices or in a central host controller [2,3]. It is thus a good method for distributing control function into field devices to create control-in-the-field architecture for reducing control interval [4,5], for minimizing scheduled communication load [6,7], and for improving process safety and availability [8,9]. However, it is also possible to achieve the required function that is not available in any field devices for building the control strategy. Recently, a technique to implement FF-based feedforward hybrid control by employing basic function blocks in field instruments and advanced function block in the host controller has been suggested [10]. This proposed control implementation is based on the utilization of the proportional-integral-derivative (PID) function block that supports internally the feedforward algorithm. The feedforward input after dynamic compensation by using a lead/lag (LL) function block is applied to combining feedback algorithm inside the PID block. Alternatively, the PID and LL blocks for configuring the FF-based feedforward control can be also located in an H1 interface card of the host system for

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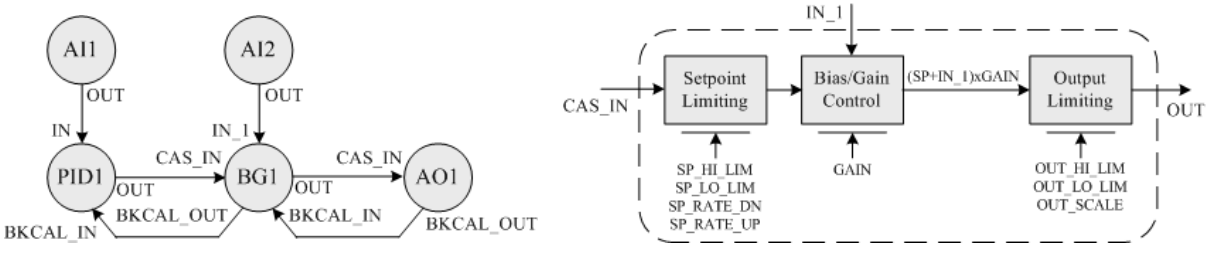
synchronization of measurement, calculation, and control with scheduled data transfers [11]. Nevertheless, both automatic feedback algorithm and feedforward contribution will be lost when setting the operating mode of the PID block to be manual (MAN) mode. In some applications to provide the operator accessibility and visibility during startup and abnormal operations, the feedforward control is still required to continue for correcting process disturbance in case of placing the PID block in MAN mode. In order to obtain this requirement, the feedforward correction must be performed outside the PID function block [12]. However, there is no practical guideline for configuring this alternative control strategy to yield minimum field-level network load for scheduled data transfers during segment macrocycle. The goal of this paper is therefore to propose a useful suggestion for selecting the placements of function blocks used for alternate FF-based feedforward implementation to provide the good performance for correcting the process disturbance input. The macrocycle schedules obtained from all possible different configuration schemes for creating the interested control by using the bias/gain (BG) function block to fulfill external feedforward summing function are examined. A temperature control loop performed from the DetlaV distributed control system (DCS) with built-in ability to run function blocks in H1 interface module is utilized as an explanatory case study for investigating how different function block placements and synchronizations affect measured disturbance corrections.

The remainder of this paper is structured as follows. An alternative of feedforward implementation using FF technology and a case study on temperature control are provided in Section 2 and Section 3, respectively. The proposed segment macrocycle analysis is described in Section 4, and experimental results are shown in Section 5. The final conclusions and possible direction for future work are given in Section 6.

2. **Alternative of FF-Based Feedforward Control.** One of major limitations of single-loop PID feedback control is that the feedback is incapable of correcting an error between the setpoint and the controlled parameter at the time of detection. This means that the process disturbance input must impact the controlled parameter before control actions can begin to correct upsets that already occurred in the system. To minimize this limitation, the feedforward correction in conjunction with feedback algorithm can be applied to anticipating the impact of measured disturbance input. The PID function blocks in FF H1 instruments and in many integrated DCS hosts support a feedforward input that combines feedback strategy. The feedforward algorithm can thus be done internally within the PID block [10,11]. In order to achieve the feedforward summing function to be outside the PID function block, one possible alternative of FF-based feedforward control loop is shown in Figure 1(a) [12]. This implementation using the BG block allows the feedforward correction to continue to perform when the PID block operation is in MAN mode. The analog input AI1 block is employed to condition the measured values of the



(a) Function block diagram (b) Internal structure of BG block

FIGURE 1. Alternative of FF-based feedforward control by using BG block

controlled parameter to be available for the PID1 block by linking to the primary input (IN), while the AI2 function block is utilized to condition the measured values of the disturbance input to be available for the BG1 block by connecting to the input (IN_1). The PID1 block output (OUT) is applied to being the bias setpoint of the BG1 block through the link to the cascade input (CAS_IN). The BG1 block calculates its output from the bias setpoint, the feedforward input, and a gain value (GAIN) as displayed in Figure 1(b). The sum of the PID output and feedforward signal is multiplied by the GAIN parameter, and then the output of the BG block becomes the cascade input of the analog output AO1 block. The connection between the BKCAL_OUT and BKCAL_IN parameters is used for providing bumpless transfer and anti-reset windup. Table 1 provides the normal operating mode and functional description of the function blocks used for alternative implementation of feedforward control as shown in Figure 1(a), where AUTO and CAS denote the automatic mode and cascade mode on the block operation, respectively.

TABLE 1. Description of function blocks used in Figure 1(a)

Block	Normal Mode	Functional Description
AI1	AUTO	Converting the measured values of the controlled variable from the transducer block within the primary transmitter to become the PID1 input.
AI2	AUTO	Converting the measured values of the disturbance input from the transducer block within the secondary transmitter to become the BG1 input.
PID1	AUTO	Calculating the control output by using the proportional, integral and derivative terms.
BG1	CAS	Computing the block output from the bias setpoint, block input, and a gain value.
AO1	CAS	Passing the BG1 output to the transducer block within the final element for regulating the controlled process.

3. **Case Study on Temperature Control.** Figure 2 depicts the case study of the temperature control with feedforward strategy for the FF H1 segment using trunk-and-spur tree topology. The controlled variable and process disturbance are the temperature produced by a 100 W lamp and temperature produced by an on/off fan, respectively. The studied control system at field level consists of three FF H1 devices (TIT_201 modeled Rosemout 3144P, TIT_202 modeled Yokogawa YTA320, and DIY_201 modeled Smar FI302) and one power regulator (TY_201 modeled Sangi Electric SCR-1A030). Table 2 summarizes the major details of the FF H1 devices of Figure 2 as well as the number of AI, PID, and AO function blocks contained in these instruments and the execution time of each block. It should be noted that the time period for executing the function block is specified by the device manufacturer. The controlled variable from 40°C to 60°C and disturbance input from 20°C to 60°C are precisely measured by the TIT_201 and TIT_202 temperature transmitters, respectively. The FF H1 fieldbus signal is converted into the 4-20 mA current by the DIY_201 converter to apply the TY_201 power regulator, which is employed as the final control element for adjusting the lamp power supply to change the heat process condition. The interested FF H1 segment is connected to the DeltaV DCS (version 10.3.2) at host level via the H1 interface card modeled Series 2. The DeltaV host used provides the functionality to assign the function blocks to be executed in the H1 interface card.

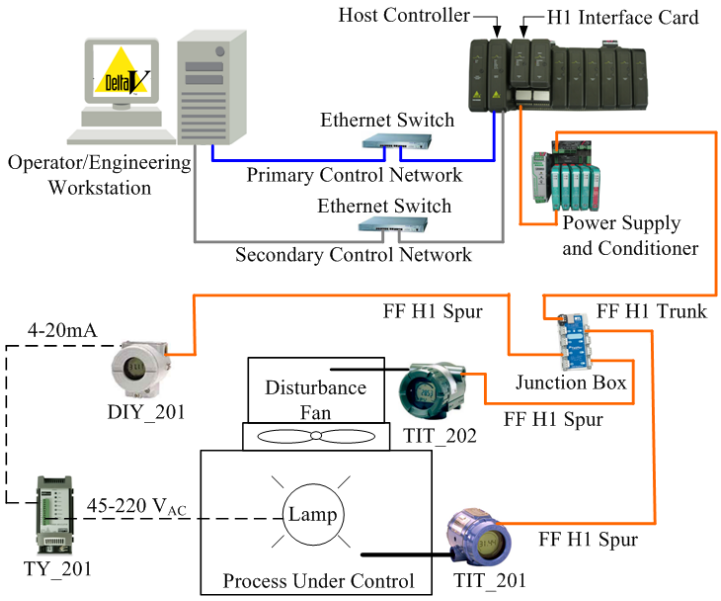


FIGURE 2. Case study on temperature control loop connected to the DeltaV host

TABLE 2. Major details of FF H1 devices of Figure 2

Item	TIT_201	TIT_202	DIY_201
Device Model	Rosemount 3144P	YTA320	FI302
Device Revision	2	2	4
Manufacturer	Emerson	Yokogawa	Smar
Number of AI blocks	3	4	N/A
Execution Time of AI block	60 ms	50 ms	N/A
Number of PID blocks	2	2	1
Execution Time of PID block	90 ms	100 ms	67 ms
Number of AO blocks	N/A	N/A	3
Execution Time of AO block	N/A	N/A	50 ms

4. **Proposed Analysis of Macrocycle Schedules.** To investigate how different function block assignments for control configuration of the alternative implementation of FF-based feedforward control by using BG block affect the segment macrocycle schedules and function block synchronizations, there are eight possible configuration schemes as given in Table 3. The AI function blocks within the TIT_201 and TIT_202 are fixed to perform the AI1 and AI2 blocks, respectively, for measurements of the controlled variable and input disturbance of the studied system. The PID function block located at the H1 field devices used, DCS host controller, or H1 interface can be selected to execute the PID1 block, while the BG function block inside either the DCS controller or H1 card can be preferred to conduct the BG1 block for feedforward summation. The AO function block allocated in the DIY_201 is fixed to act the AO1 block for conversion of the FF data into 4-20 mA signal to supply the TY_201. The Control Studio application of the DeltaV DCS was utilized for building the control loop of Figure 1(a) by differently assigning the function blocks within the control module named 'FEEDFORWARD_BG'. Based on FF technology, the function blocks used to build control strategy for the FF H1 segment are executed according to the macrocycle schedule generated by the host configuration

TABLE 3. Possible configurations for building feedforward loop of Figure 1(a)

Scheme	AI1	AI2	PID1	BG1	AO1
1	TIT_201	TIT_202	TIT_201	DCS Controller	DIY_201
2	TIT_201	TIT_202	TIT_202	DCS Controller	DIY_201
3	TIT_201	TIT_202	DIY_201	DCS Controller	DIY_201
4	TIT_201	TIT_202	DCS Controller	DCS Controller	DIY_201
5	TIT_201	TIT_202	Interface Card	Interface Card	DIY_201
6	TIT_201	TIT_202	TIT_201	Interface Card	DIY_201
7	TIT_201	TIT_202	TIT_202	Interface Card	DIY_201
8	TIT_201	TIT_202	DIY_201	Interface Card	DIY_201

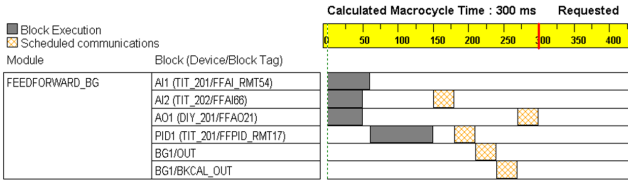
tool. The schedule also specifies the data transfer for external links between function blocks located in different devices. The time interval of 30 ms is spent on each scheduled data transfer. From Schemes 1-4 by allocation of the BG1 block in the DCS controller, the execution time of this block is excluded in each of the segment macrocycle schedules as shown in Figures 3(a)-3(d), respectively. It is seen that the processing of the BG1 block assigned in the DCS host controller is not synchronized with the processing of other function blocks placed in H1 field devices. Conversely, from Schemes 5-8 by allocation of the BG1 block in the H1 interface card, the execution time of this block is included in each of the schedules as shown in Figures 3(e)-3(h), respectively. It can be seen that the execution of BG1 block assigned in the H1 interface card is fully synchronized with the executions of other function blocks assigned in H1 field devices. In the same way, from Scheme 4 by placing the PID1 block in the DCS controller, its execution time is excluded in the macrocycle schedule (see Figure 3(d)), whereas from Scheme 5 by placing the PID1 block in the H1 card, its execution time is included in the macrocycle schedule (see Figure 3(e)). A control interval (C_{intv}) for the control loop, related to the calculated macrocycle, can be expressed as [4]

$$C_{\text{intv}} = \sum_{i=1}^{N} C_{\text{block\_}i} + \sum_{j=1}^{M} C_{\text{sched\_}j} + C_{\text{margin}} \tag{1}$$

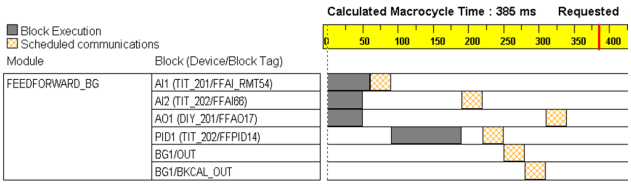
where $C_{\text{block\_}i}$ and $C_{\text{sched\_}j}$ are the time periods required by the ith task of function block executions and the jth task of scheduled data communications, respectively, N is the number of block execution tasks, M is the number of scheduled communication tasks, and C_{margin} denotes the margin time defined by the system configurator to confirm the completion of both execution and communication tasks contained by the control interval. Based on full function block synchronizations of Schemes 5-8, the macrocycle schedules are optimized by the control loop latency minimization from scheduling the function block execution and scheduled communication tasks in parallel whenever possible. For example in Figure 3(g), the AI1 and AI2 blocks are executed simultaneously, and the execution of the PID1 block is processed concurrently with the scheduled data transfer from the AI2 block output to the BG1 block input. Therefore, the control interval for Scheme 7 ($C_{\text{intv\_Scheme7}}$) in case of $M = 5$ can be given by

$$\begin{aligned} C_{\text{intv\_Scheme7}} &= C_{\text{AI1}} + 30\text{ms} + C_{\text{PID1}} + 30\text{ms} + C_{\text{BG1}} + 30\text{ms} + C_{\text{AO1}} \\ &\quad + 30\text{ms} + 30\text{ms} + C_{\text{margin}} \\ &= C_{\text{AI1}} + C_{\text{PID1}} + C_{\text{BG1}} + C_{\text{AO1}} + C_{\text{margin}} + (5 \times 30\text{ms}) \end{aligned} \tag{2}$$

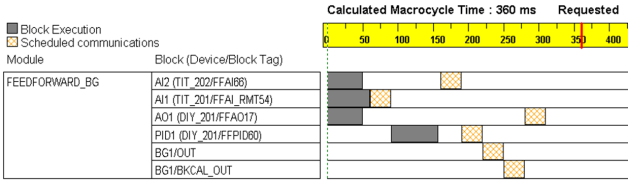
where C_{AI1}, C_{PID1}, C_{BG1}, and C_{AO1} are the execution times of the AI1, PID1, BG1, and AO1 function blocks, respectively. Table 4 shows the number of external function block



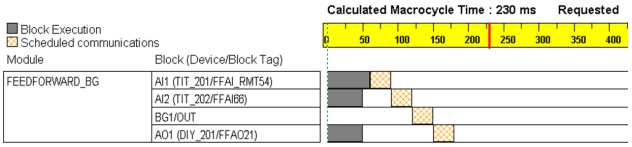
(a) Scheme 1



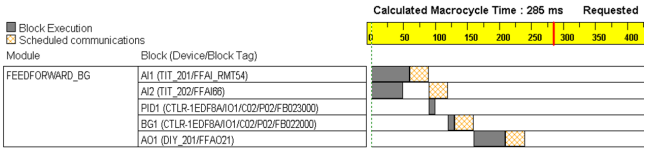
(b) Scheme 2



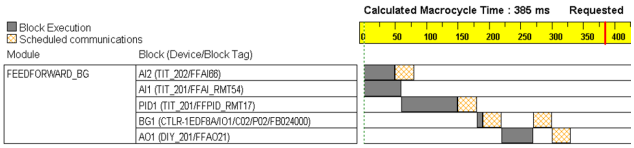
(c) Scheme 3



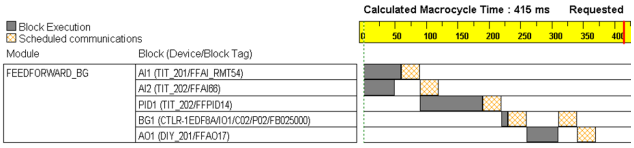
(d) Scheme 4



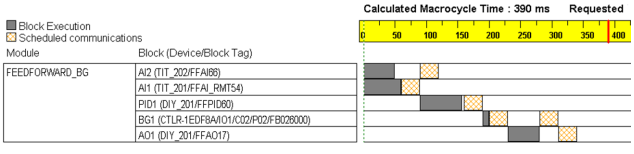
(e) Scheme 5



(f) Scheme 6



(g) Scheme 7



(h) Scheme 8

FIGURE 3. Schedules generated for different control configurations of Table 3

TABLE 4. Calculated macrocycle times and network traffic loads

Scheme	Number of External Links	Calculated Macrocycle	Network Load	Communications and Block Executions
1	5	300 ms	50.00%	Non-Synchronization
2	6	385 ms	46.75%	Non-Synchronization
3	6	360 ms	50.00%	Non-Synchronization
4	4	230 ms	52.17%	Non-Synchronization
5	4	285 ms	42.10%	Synchronization
6	5	385 ms	38.96%	Synchronization
7	6	415 ms	43.37%	Synchronization
8	6	390 ms	46.15%	Synchronization

links, the calculated macrocycle time, and the network traffic load for scheduled communications during each of the calculated macrocycles of Figures 3(a)-3(h). It is evident that the function block assignment for control configuration affects not only the interval of calculated macrocycle and the percentage of network load but also the synchronization of function block executions and communications. The configurations of Schemes 4 and 6 provide the maximum and minimum network traffic loads for scheduled data transfers, respectively.

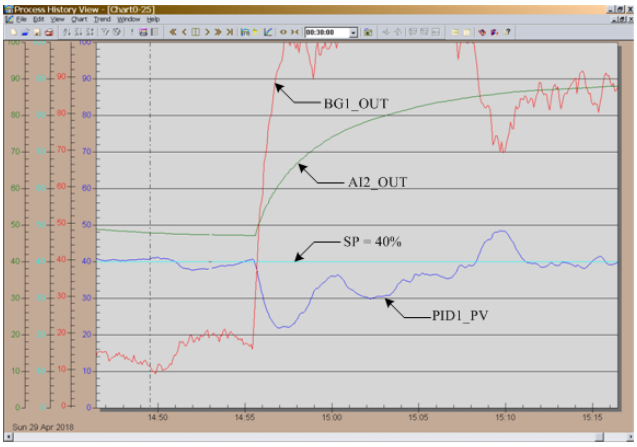
5. **Experimental Results.** There are two macrocycle schedule options for operating the FF H1 segment on the DeltaV system. The first is a module-driven option for providing the calculated macrocycle to individually specify the scan rate for each function block, and the latter is a user-specified option for providing the requested macrocycle to execute all function blocks at the same scan rate. The DeltaV DCS host employs the greater of the calculated or requested macrocycle to decide the actual macrocycle schedule.

To coordinate the rate of executing the created control module with the segment macrocycle in practical experiments, the second schedule option was selected by defining the requested macrocyele to be 1 s. In order to compare the control performances for anticipating disturbance effects, the control strategy configurations of Schemes 4, 5, and 6 by assigning the PID function block to the DCS host controller, H1 interface card, and TIT_201 temperature transmitter, respectively, were utilized to build the control loop of Figure 1(a). The control parameters of the PID1 block are GAIN = 1.4, RESET = 99.2 s, and RATE = 18.5 s. The gain parameter of the BG1 block is GAIN = 0.8. Figures 4(a), 4(b), and 4(c) show the responses under the disturbance caused by fan operation for the setpoint (SP) of 40% from configuring the alternative of feedforward control by using Scheme 4 (with the recovery time of 21.55 min), Scheme 5 (with the recovery time of 20.49 min), and Scheme 6 (with the recovery time of 16.00 min), respectively. It is clearly seen that different function block placements of control strategy configuration affect the measured disturbance correction of feedforward algorithm.

6. **Conclusions.** An alternative of FF-based feedforward control by using bias/gain function block for performing external feedforward summing function has been described. The analysis of the segment macrocycles generated for this alternative implementation has been presented. The temperature control of FF H1 segment operating in the DeltaV integrated host has been utilized as the exegetical case study for analyzing the effects of different control strategy configurations by differently assigning function blocks as well as for comparing the performances of the control loop built by the selected configuration

(a) Scheme 4 by placing the PID block in the DCS host controller

(b) Scheme 5 by placing the PID block in the H1 interface card



(c) Scheme 6 by placing the PID block in the TIT_201 transmitter

FIGURE 4. Disturbance responses

schemes. The future work is an analysis of possible availability and safety improvements of the studied feedforward control.

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