

DESIGN AND EXPERIMENTAL EVALUATION OF A STACKED DICKSON MULTIPLIER FOR SHOCKWAVE NON-THERMAL FOOD PROCESSING

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ABSTRACT. *This paper proposes a stacked Dickson multiplier (SDM) for non-thermal food processing utilizing underwater shockwaves. Unlike conventional high voltage multipliers, the proposed multiplier has SDM topology with a driver circuit generating high speed rectangular pulses. The SDM topology enables the proposed multiplier to achieve high voltage gains, low capacitor voltage stress, and high-speed operation by reducing the number of multiplier stages. The effectiveness of the proposed multiplier is clarified by theoretical analysis and experiments. The theoretical analysis reveals the maximum output voltage of the proposed multiplier by assuming a four-terminal equivalent model. Furthermore, the experimental results demonstrate that the proposed multiplier can provide about 3.95 kV output within 107 s when the voltage gain is 24 and the input voltage is 100 V at 60 Hz.*

Keywords: Shockwave non-thermal food processing, Dickson multipliers, High voltage multipliers, Underwater shockwaves, High voltage gains, Stack topology

1. **Introduction.** Non-thermal food processing utilizing underwater shockwaves [1-4] is one of the most promising technologies for providing nutritious softened foods, where a high voltage multiplier generating about 3-4 kV output [5-8] is used to perform underwater shockwave treatment. For this reason, several types of high voltage multipliers have been proposed in past studies. Among others, the Cockcroft-Walton voltage multiplier (CWVM) [5-12] and the Dickson charge pump (DCP) [13-15] are well-known high-voltage generators. However, the output voltage of the CWVM decreases as the number of multiplier stages increases, though the CWVMs can achieve low capacitor voltage stress. On the other hand, the DCP suffers from high capacitor voltage stress, though the DCP can reduce output voltage drops. Following these studies, as a compromise of the CWVM and the DCP, the hybrid Cockcroft-Walton/Dickson (HCWD) multiplier [16] was proposed in 2020. Owing to the hybrid topology, the HCWD multiplier can achieve not only low output voltage drop but also low capacitor voltage stress. However, it is not suitable for the shockwave non-thermal food processing, because the response time of the HCWD multiplier is slow.

In this paper, a stacked Dickson multiplier (SDM) is presented for non-thermal food processing utilizing underwater shockwaves. Unlike conventional high voltage multipliers, the proposed multiplier has stack topology employing the Dickson multipliers with a driver circuit generating high speed rectangular pulses. Since the proposed multiplier driven by the high-speed clock pulses can reduce the number of multiplier stages by the stack topology, not only high voltage gains but also high-speed operation and low capacitor voltage stress can be achieved. The characteristics of the proposed multiplier are investigated by theoretical analysis and experiments.

The organization of this paper is as follows. First, we perform the research survey and clarify the problem definition of this research in this section. Next, regarding the proposed multiplier, the details of the circuit configuration and its operation principle are described in Section 2. Then, the characteristic of the proposed multiplier is clarified mathematically by theoretical analysis in Section 3. After that, the feasibility of the proposed multiplier is confirmed experimentally in Section 4. Finally, the results of this work are summarized briefly in Section 5.

2. Circuit Configuration. Figure 1 illustrates the circuit configuration of the proposed multiplier. As it can be seen from Figure 1, the proposed multiplier is composed of an isolation transformer, two full waveform rectifiers (FWRs), a pulse generator, and an SDM. First, the DC voltages V_{max} and $-V_{max}$ are obtained by the FWRs, where $|V_{max}|$ denotes the amplitude of the AC input V_{ac} . Next, by controlling IGBT switches Q1 and Q2 by the two-phase clock pulses Φ_1 and Φ_2 , the pulse generator provides high speed clock pulses to the SDM. Finally, the SDM with the voltage gain of 24 generates the output voltage 3.4 kV ($= 100 \text{ V} \times \sqrt{2} \times 24$), where the SDM consists of 6 modules with 2 multiplier stages.

In the following section, the output voltage of the proposed multiplier will be derived theoretically by using a four-terminal equivalent model [17-19].

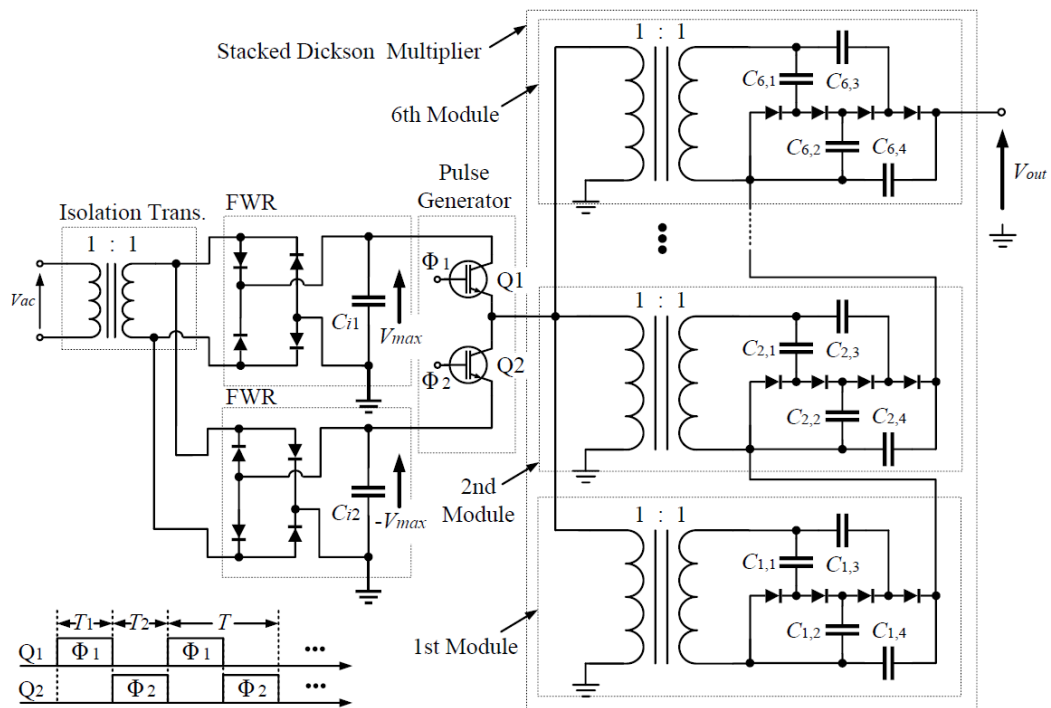


FIGURE 1. Proposed high voltage multiplier

3. Theoretical Analysis. In this section, the output voltage of the proposed multiplier is analyzed theoretically by assuming the four-terminal equivalent model, where the theoretical analysis is performed under the conditions that the time constant of the proposed multiplier is much larger than the period of Φ_1 and Φ_2 , T .

Figure 2 describes the instantaneous equivalent circuits of the proposed multiplier, where we model the diode switch by using an ideal switch, the resistance R_d , and the

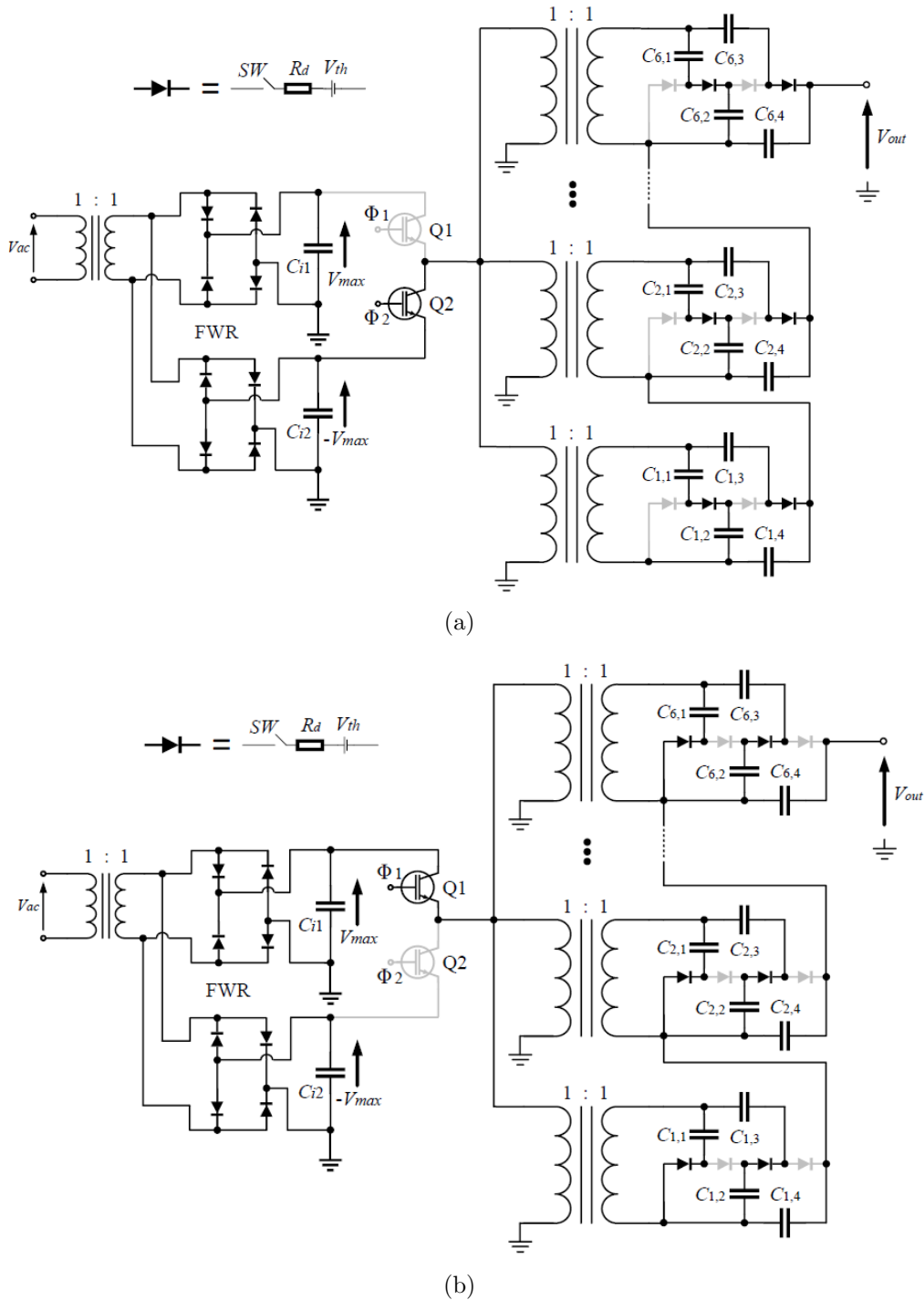


FIGURE 2. Instantaneous equivalent circuits of the proposed multiplier: (a) State- T_1 (Φ_1 is high and Φ_2 is low) and (b) State- T_2 (Φ_1 is low and Φ_2 is high)

threshold voltage V_{th} . Applying Kirchoff's current law for Figure 2, the variation of the electric charge in the input and output terminals of the i -th ($i = 1, \dots, 6$) module, $\Delta q_{T_k, v_{in.i}}$ and $\Delta q_{T_k, v_{out.i}}$ ($k = 1, 2$), can be obtained as

$$\Delta q_{T_1, v_{in.i}} = \Delta q_{T_1}^{i,1} + \Delta q_{T_1}^{i,3}, \quad \Delta q_{T_1, v_{out.i}} = \Delta q_{T_1}^{i,4}, \quad \text{and} \quad \Delta q_{T_1}^{i,2} = -\Delta q_{T_1}^{i,3}. \quad (1)$$

$$\Delta q_{T_2, v_{in.i}} = -\Delta q_{T_2}^{i,1} - \Delta q_{T_2}^{i,3}, \quad \Delta q_{T_2, v_{out.i}} = \Delta q_{T_2}^{i,3} + \Delta q_{T_2}^{i,4}, \quad \text{and} \quad \Delta q_{T_2}^{i,2} = -\Delta q_{T_2}^{i,4}. \quad (2)$$

In (1) and (2), $\Delta q_{T_k}^{i,j}$ ($j = 1, 2, 3, 4$) is the variation of electric charge in the j -th capacitor, where the sum of the variations in $\Delta q_{T_k}^{i,j}$ is zero at a steady state condition. Substituting (1) and (2) for

$$I_{in.i} = (\Delta q_{T_1, v_{in.i}} + \Delta q_{T_2, v_{in.i}}) / T \quad \text{and} \quad I_{out.i} = (\Delta q_{T_1, v_{out.i}} + \Delta q_{T_2, v_{out.i}}) / T, \quad (3)$$

we have

$$I_{in.i} = -4 I_{out.i}. \quad (4)$$

In (3), $I_{in.i}$ and $I_{out.i}$ are the average input and output currents of the i -th module, respectively. From (4), the voltage gain of the i -th module, m_i , is obtained as 4.

Next, the power loss of the i -th module is discussed to calculate the internal resistance R_{SC_i} . From Figure 2, the power loss of the i -th module, W_{T_i} , is expressed as

$$W_{T_i} = W_{T_{1.i}} + W_{T_{2.i}}, \quad (5)$$

$$\begin{aligned} \text{where } W_{T_{1.i}} &= \frac{R_d}{T_1} (\Delta q_{T_1}^{i,1})^2 + \frac{R_d}{T_1} (\Delta q_{T_1}^{i,3})^2 \\ \text{and } W_{T_{2.i}} &= \frac{R_d}{T_2} (\Delta q_{T_2}^{i,1})^2 + \frac{R_d}{T_2} (\Delta q_{T_2}^{i,3})^2. \end{aligned} \quad (6)$$

In (5) and (6), $W_{T_{k.i}}$ is the power loss in State- T_k . Rearranging (5) and (6), the power loss is obtained as

$$W_{T_i} = 8R_d(I_{out.i})^2T, \quad (7)$$

because $T_1 = T_2 = T/2$. Therefore, we have the internal resistance R_{SC_i} as $8R_d$. Using m_i and R_{SC_i} , the equivalent model of the i -th module can be expressed by the following K-matrix [18,19]:

$$\begin{bmatrix} |V_{\max}| - V_{th} \\ I_{in.i} \end{bmatrix} = \begin{bmatrix} \frac{1}{4} & 0 \\ 0 & 4 \end{bmatrix} \begin{bmatrix} 1 & 16R_t + 8R_d \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{out.i} \\ -I_{out.i} \end{bmatrix}, \quad (8)$$

where R_t denotes the internal resistance of the transformer. From (8), the equivalent model of the proposed multiplier can be expressed as Figure 3. In other words, the equivalent model of the proposed multiplier is given as

$$\begin{bmatrix} |V_{\max}| - V_{th} \\ I_{in} \end{bmatrix} = \begin{bmatrix} \frac{1}{24} & 0 \\ 0 & 24 \end{bmatrix} \begin{bmatrix} 1 & 96R_t + 48R_d \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{out} \\ -I_{out} \end{bmatrix}. \quad (9)$$

Finally, from (9), we can obtain the maximum output voltage of the proposed multiplier as

$$V_{out} = 24 (|V_{\max}| - V_{th}) \times \left(\frac{R_L}{R_L + 96R_t + 48R_d} \right), \quad (10)$$

where R_L denotes an output load. As it can be seen from (10), the output voltage becomes $24(|V_{\max}| - V_{th})$ if the internal resistance $96R_t + 48R_d$ is much smaller than R_L . Hence, the output voltage of the proposed multiplier is about 3.4 kV for the 100 V AC input.

The feature comparisons between the proposed multiplier and the conventional state-of-the-art multipliers proposed in [5-7,16] are demonstrated in Table 1. In this comparison, the proposed multiplier was compared with the conventional Cockcroft-Walton Type

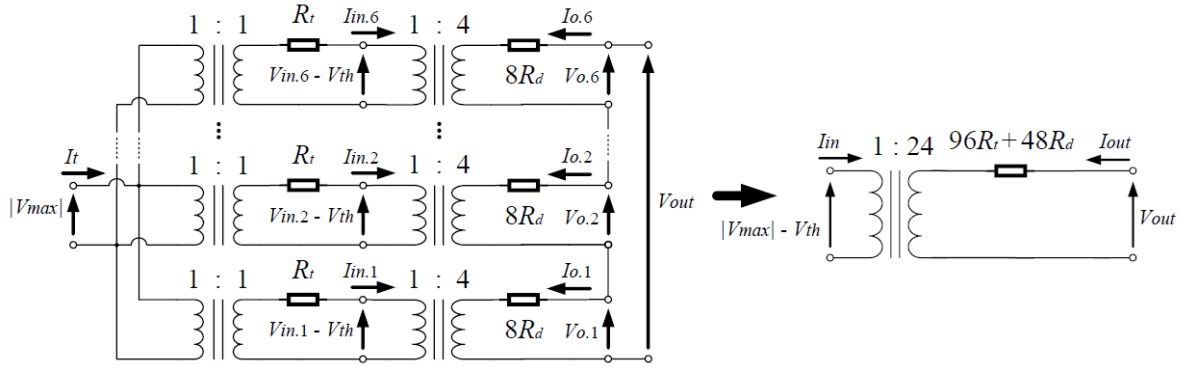


FIGURE 3. Equivalent circuit of the proposed voltage multiplier

TABLE 1. Feature comparisons of high voltage multipliers

	Topology	Gain	Speed	Voltage stress
Conventional [5] (2017)	Bipolar Cockcroft-Walton multiplier using switched-capacitor AC-AC converter	26	Slow	$8V_{\max}$
Conventional [6] (2018)	Series-connected bipolar Cockcroft-Walton multiplier	28	Fast	$8V_{\max}$
Conventional [7] (2020)	Modified series-connected bipolar voltage multiplier (HVM-B)	28	Fast	$8V_{\max}$
Conventional [16] (2020)	Hybrid Cockcroft-Walton/Dickson multiplier (2 stages \times 6 cells)	24	Slow	$4V_{\max}$
Proposed	Stacked Dickson multiplier	24	Fast	$4V_{\max}$

multipliers, because the traditional Dickson charge pump has a serious drawback in the voltage stress of circuit components. In high voltage applications, the traditional Dickson charge pump requires circuit components with a high withstand voltage. As Table 1 shows, both high speed operation and low voltage stress are achieved by the proposed multiplier. Furthermore, without increasing the number of multiplier stages, the proposed multiplier can provide higher voltage gains by increasing the number of modules.

4. Experiment. In this section, the feasibility of the proposed multiplier is confirmed experimentally. In this experiment, the laboratory prototype shown in Figure 4 was assembled by the diode 1N4007, the driver IC IR2110PBF, the IGBT GT50JR22, and the film capacitor $1 \mu\text{F}$, where the frequency of Φ_1 and Φ_2 was set to 10 kHz.

Figure 5 demonstrates the measured output voltage of the experimental circuit for the input voltage 100 V at 60 Hz, where the proposed multiplier was compared with the conventional multiplier [6] under the input voltage 100 V at 60 Hz. In this figure, the output terminal of the proposed multiplier was connected to the big capacitor produced by TOEI corporation, where the capacitance is $200 \mu\text{F}$ and the rated voltage is 4000 V DC. As Figure 5 shows, the proposed multiplier provides about 3.95 kV within 107 s. On the other hand, the conventional multiplier [6] generates about 3.93 kV within 281 s. Therefore, the proposed multiplier is faster than conventional multiplier. Figure 6 shows the measured output current of the proposed multiplier. As this figure shows, the maximum current between the electrodes during the discharging process is 23 kA.

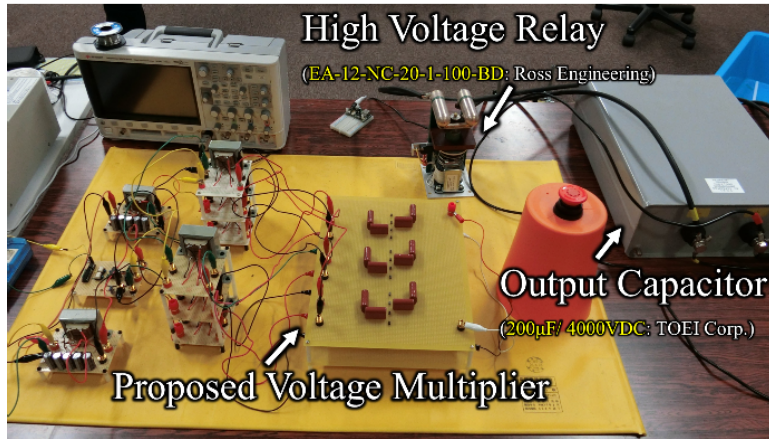


FIGURE 4. Shockwave non-thermal food processing system using the proposed multiplier with a 200 μF output capacitor

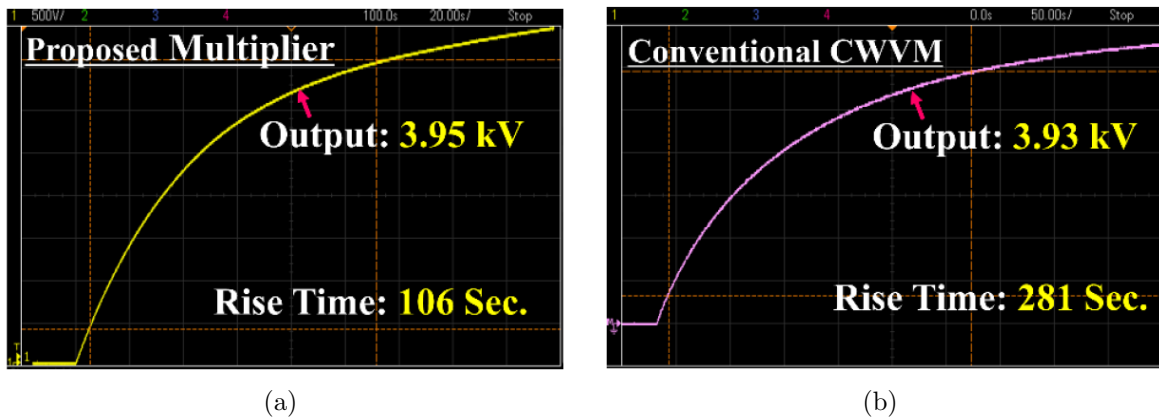


FIGURE 5. Measured output voltage: (a) Proposed multiplier and (b) conventional CWVM proposed in [6]

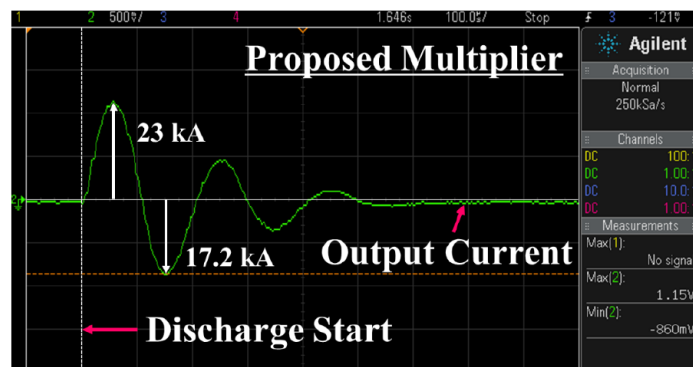


FIGURE 6. Measured output current of the proposed multiplier

5. **Conclusions.** For non-thermal food processing systems utilizing underwater shockwaves, an SDM has been proposed in this paper. Unlike conventional high voltage multipliers, the proposed multiplier has stack topology employing the Dickson multipliers with a driver circuit generating high speed rectangular pulses.

By assuming a four-terminal equivalent model, theoretical analysis clarified the maximum output voltage of the proposed multiplier mathematically. Furthermore, the feasibility of the proposed multiplier was confirmed by laboratory experiments. In the performed experiments, the output voltage of the proposed multiplier reached about 3.95 kV within 107 s by converting a 100 V at 60 Hz input. From these obtained results, the proposed multiplier can achieve a voltage gain of 24 at high speed.

In future research, we are going to assemble the shockwave non-thermal food processing system by using the proposed multiplier and perform shockwave non-thermal food processing.

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