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SIMULATION AND ANALYSIS OF A MULTIPLE-INPUT SINGLE-OUTPUT AC/DC CONVERTER FOR 13.56 MHZ WIRELESS POWER TRANSFER SYSTEMS

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Abstract. *For 13.56 MHz wireless power transfer (WPT) systems, a multiple-input single-output (MISO) AC/DC converter is proposed in this paper. To supply DC voltage from small vibration inputs such as 1 V, 12 times gain is realized by the proposed converter. Unlike conventional converters, the proposed MISO converter has the hybrid Cockcroft-Walton/Dickson (HCWD) topology. The MISO HCWD topology enables the proposed converter to achieve high gain with low voltage stress. To clarify the effectiveness of the proposed converter, theoretical analysis and computer simulations are performed by using the simulation program with integrated circuit emphasis (SPICE) simulator. The result of the computer simulations showed that the proposed converter can provide a DC output from 1 V at 13.56 MHz input, where the power efficiency reaches 67% with an output power of 10 mW. Furthermore, the comparison between the proposed converter and the conventional converters, such as single-input single-output (SISO) Cockcroft-Walton converter, SISO Dickson converter, and SISO HCWD converter, reveals that the proposed converter can achieve excellent performance in terms of output voltage, power efficiency, voltage gain, and ripple factor.*

Keywords: Wireless power transfer systems, Hybrid AC/DC converters, Cockcroft-Wanton converters, Dickson converters, Multiple-input single-output topologies

1. **Introduction.** In the design of wireless power transfer (WPT) systems [1-4], an AC/DC converter [5-7] is one of the most important components for converting the AC voltage provided by power receiving coils. In past studies, several types of step-up converters have been developed for the WPT system. For high-speed signal conversion, the single-input single-output (SISO) Cockcroft-Walton converter [8-10] and the SISO Dickson converter [11-13] are typical step-up AC/DC converters. Although these converters can achieve high voltage gain easily by increasing the number of multiplier stages, each conventional converter has the following drawback. In the Cockcroft-Walton converter [8-10], the output voltage begins to drop as the number of multiplier stages increases. Therefore, the Cockcroft-Walton converter is low power efficiency when achieving high voltage gains. On the other hand, the Dickson converter [11-13] suffers from high voltage stress when achieving high voltage gains. Furthermore, Fibonacci type converters [14-17], a family of the Dickson converters, also have a problem with voltage stress. As a

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compromise of these traditional converters, the SISO hybrid Cockcroft-Walton/Dickson (HCWD) converter was recently proposed [18,19]. The SISO HCDW converter has intermediate characteristics between the traditional SISO converters. Namely, the internal resistance of the SISO HCWD converter is smaller than the SISO Cockcroft-Walton converter and larger than the SISO Dickson converter. Furthermore, the voltage stress of the SISO HCWD converter is larger than the SISO Cockcroft-Walton converter and smaller than the SISO Dickson converter. However, there is still room for improvement in the converter topology.

In this paper, we present a multiple-input single-output (MISO) [20-22] AC/DC converter with HCWD topology [18,19]. To supply high DC voltage from small vibration inputs such as 1 V at 13.56 MHz, the proposed converter provides 12 times gain. The key idea of the proposed converter is the combination of HCWD topology and MISO topology. The proposed MISO HCWD topology allows to achieve lower voltage stress and higher power efficiency than the SISO HCWD converter. Furthermore, by increasing the number of modules, the proposed converter can provide higher gain easily. The characteristics of the proposed converter are investigated by theoretical analysis and computer simulations.

The rest of this paper is organized as follows. First, the circuit configuration of the proposed converter and its operating principle are described in Section 2. Next, the properties of the proposed converter are analyzed theoretically in Section 3. Then, the effectiveness of the proposed converter is justified by computer simulations in Section 4, where the comparison is performed between the proposed converter and conventional converters. Finally, the results of this research are summarized briefly in Section 5.

2. **Circuit Configuration.** Figure 1 illustrates the circuit configuration of the proposed MISO AC/DC converter realizing 12 times gain. As this figure shows, the proposed converter consists of a series-connection of two modules, where each module provides 6 times gain. Unlike conventional SISO AC/DC converters for 13.56 MHz wireless power transfer (WPT) systems, the proposed converter is a MISO converter with the HCWD topology. The operation of each module is as follows.

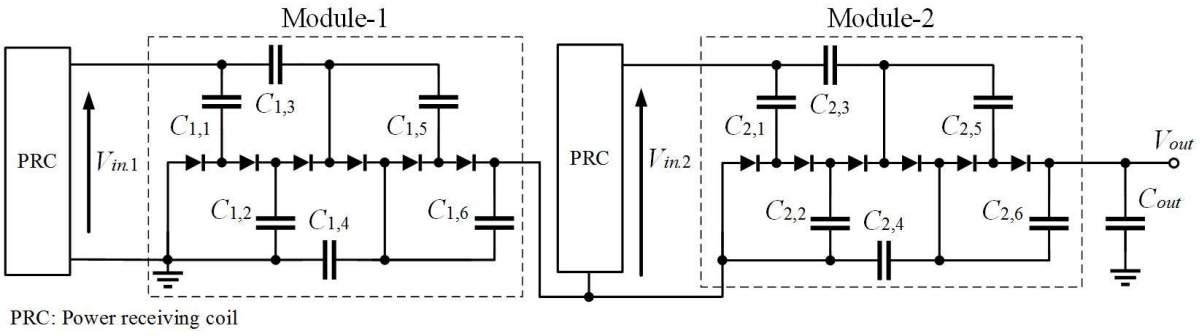


FIGURE 1. Proposed MISO AC/DC converter with HCWD topology

Figure 2 depicts the instantaneous equivalent circuit of the i-th module, where state-T_n is the state when $V_{in.i}$ $(i = 1, 2)$ is negative and state-T_p is the state when $V_{in.i}$ is positive. In these figures, $\Delta q_{T_n,V_{in.i}}$ and $\Delta q_{T_p,V_{in.i}}$ are the changes in the charge of the input terminal. On the other hand, $\Delta q_{T_n,V_{out.i}}$ and $\Delta q_{T_p,V_{out.i}}$ are the changes in the charge of the output terminal. To simplify the explanation of circuit operation, the input voltage $V_{in.i}$ is assumed to be a rectangular waveform with a duty cycle of 0.5, and the diode is modelled by a series-connection of a lossless switch, an internal resistance R_d, and a threshold voltage V_{th}. In steady state under these assumptions, the voltage of the capacitors $C_{i,j}$ $(j = 1, \ldots, 6)$, $V_{C_{i,j}}$, becomes $V_{C_{i,1}} = |V_{\max.i}|$, $V_{C_{i,2}} = V_{C_{i,5}} = V_{C_{i,6}} =$

$2|V_{\max.i}|$, $V_{C_{i,3}} = 3|V_{\max.i}|$, and $V_{C_{i,4}} = 4|V_{\max.i}|$, where $|V_{\max.i}|$ is the amplitude of $V_{in.i}$. Therefore, the output voltage of each module, $V_{out.i}$, is expressed as

$$V_{out.i} \cong 6(|V_{\max.i}| - V_{th}). \tag{1}$$

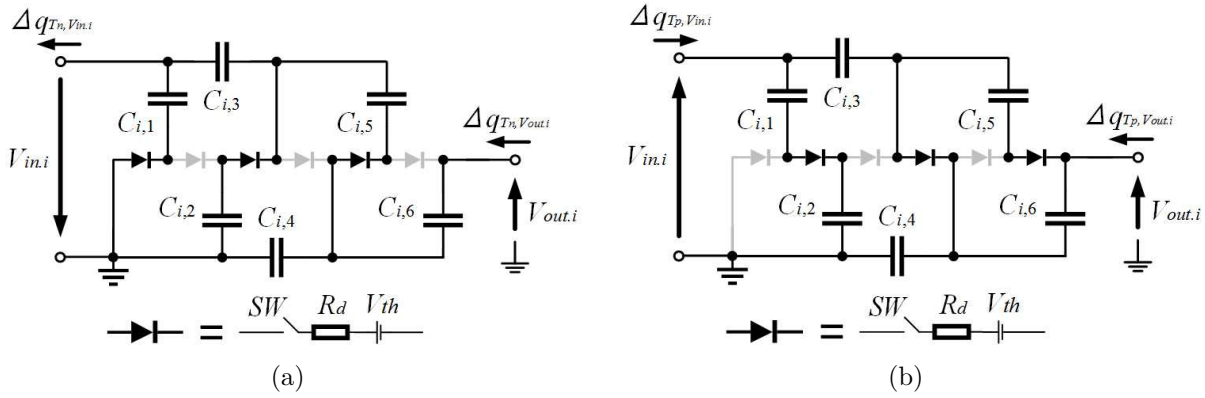


FIGURE 2. Instantaneous equivalent circuit of the i-th module ($i = 1, 2$): (a) state-T_n and (b) state-T_p

By the series-connection of two modules, the proposed converter provides

$$V_{out} \cong 6\sum_{i=1}^{2}(|V_{\max.i}| - V_{th}). \tag{2}$$

Of course, the proposed converter can achieve higher voltage gain by increasing the number of modules or the number of multiplier stages within the module.

3. **Theoretical Analysis.** The properties of the proposed converter shown in Figure 1 are analyzed theoretically. In this analysis, the characteristics of the proposed converter, maximum output voltage and maximum power efficiency, are formulated by using a four-terminal model [23,24].

First, the conversion ratio m_i and the internal resistance R_{SC_i} of the i-th module are analyzed to obtain the four-terminal model of the proposed converter. If a time constant of the i-th module is much larger than the period of $V_{in.i}$, changes in the charge of $C_{i,j}$, $\Delta q_{T_n}^{i,j}$ and $\Delta q_{T_p}^{i,j}$, satisfy

$$\Delta q_{T_n}^{i,j} + \Delta q_{T_p}^{i,j} = 0. \tag{3}$$

In state-T_n, changes in the charge of I/O terminals, $\Delta q_{T_n,V_{in.i}}$ and $\Delta q_{T_n,V_{out.i}}$, are derived by applying the Kirchhoff's current law as follows:

$$\Delta q_{T_n,V_{in.i}} = \Delta q_{T_n}^{i,1} + \Delta q_{T_n}^{i,3} \text{ and } \Delta q_{T_n,V_{out.i}} = \Delta q_{T_n}^{i,6}, \tag{4}$$

$$\text{where } \Delta q_{T_n}^{i,3} = -\Delta q_{T_n}^{i,2} + \Delta q_{T_n}^{i,5} \text{ and } \Delta q_{T_n}^{i,6} = \Delta q_{T_n}^{i,4} + \Delta q_{T_n}^{i,5}. \tag{5}$$

On the other hand, in state-T_p, changes in the charge of I/O terminals, $\Delta q_{T_p,V_{in.i}}$ and $\Delta q_{T_p,V_{out.i}}$ are obtained as

$$\Delta q_{T_p,V_{in.i}} = -\Delta q_{T_p}^{i,1} - \Delta q_{T_p}^{i,3} \text{ and } \Delta q_{T_p,V_{out.i}} = \Delta q_{T_p}^{i,5} + \Delta q_{T_p}^{i,6}, \tag{6}$$

$$\text{where } \Delta q_{T_p}^{i,1} = -\Delta q_{T_p}^{i,2} \text{ and } \Delta q_{T_p}^{i,5} + \Delta q_{T_p}^{i,6} = \Delta q_{T_p}^{i,3} + \Delta q_{T_p}^{i,4}. \tag{7}$$

Using (4) and (6), the average I/O currents are expressed as

$$I_{in.i} = \left(\Delta q_{T_n,V_{in.i}} + \Delta q_{T_p,V_{in.i}}\right)/T \text{ and } I_{out.i} = \left(\Delta q_{T_n,V_{out.i}} + \Delta q_{T_p,V_{out.i}}\right)/T. \tag{8}$$

In this equation, T is a period of $V_{in.i}$ that satisfies $T = T_n + T_p$ ($T_n = T_p$). Substituting (3)-(7) for (8), we get

$$I_{in.i} = -6I_{out.i}. \tag{9}$$

Therefore, the conversion ratio m_i is obtained as 6. Next, the internal resistance R_{SC_i} will be obtained by calculating conduction loss W_{T_i}. The total condition loss of the instantaneous equivalent circuits shown in Figure 2 is expressed as

$$W_{T_i} = W_{T_{n.i}} + W_{T_{p.i}}, \tag{10}$$

$$\text{where} \quad W_{T_{n.i}} = \frac{R_d}{T_n}\left(\Delta q_{T_n}^{i,1}\right)^2 + \frac{R_d}{T_n}\left(\Delta q_{T_n}^{i,2}\right)^2 + \frac{R_d}{T_n}\left(\Delta q_{T_n}^{i,5}\right)^2 \tag{11}$$

$$\text{and} \quad W_{T_{p.i}} = \frac{R_d}{T_p}\left(\Delta q_{T_p}^{i,1}\right)^2 + \frac{R_d}{T_p}\left(\Delta q_{T_p}^{i,5}\right)^2 + \frac{R_d}{T_p}\left(\Delta q_{T_p}^{i,5} - \Delta q_{T_p}^{i,3}\right)^2. \tag{12}$$

In these equations, $W_{T_{n.i}}$ and $W_{T_{p.i}}$ are the conduction losses in state-T_n and state-T_p, respectively. Substituting (3)-(7) for (10)-(12), W_{T_i} is rewritten as

$$W_{T_i} = \frac{12R_d}{T}\left(\Delta q_{V_{out.i}}\right)^2. \tag{13}$$

Therefore, R_{SC_i} is obtained as $12R_d$, because the conduction loss of the four-terminal model [23,24] is given by

$$W_{T_i} = \frac{R_{SC_i}}{T}\left(\Delta q_{V_{out.i}}\right)^2. \tag{14}$$

Combining m_i and R_{SC_i}, the four-terminal model of the proposed converter is illustrated as Figure 3. Obviously, higher voltage gain can be achieved by increasing the number of modules. Under the conditions that $|V_{\max}| = |V_{\max.1}| = |V_{\max.2}|$, Figure 3 can be expressed as

$$\begin{bmatrix} |V_{\max}| - V_{th} \\ I_{in} \end{bmatrix} = \begin{bmatrix} 1/12 & 0 \\ 0 & 12 \end{bmatrix} \begin{bmatrix} 1 & 24R_d \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{out} \\ -I_{out} \end{bmatrix}. \tag{15}$$

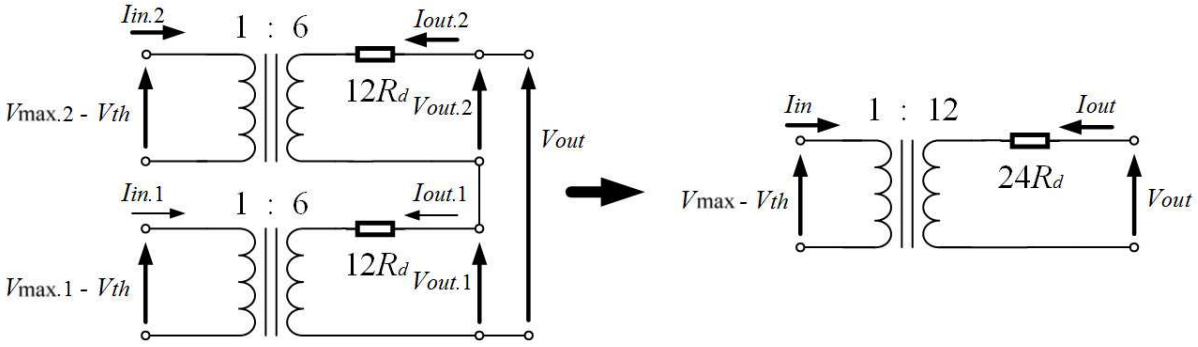


FIGURE 3. Four-terminal model of the proposed converter

Finally, we get the maximum output voltage and maximum power efficiency as

$$V_{out} = 12(|V_{\max}| - V_{th}) \times \left(\frac{R_L}{R_L + 24R_d}\right) \text{ and } \eta = \frac{R_L}{R_L + 24R_d}. \tag{16}$$

In (16), R_L denotes an output load.

4. **Evaluation through Computer Simulations.** To evaluate the characteristics of the proposed converter shown in Figure 1, computer simulations were performed by using the SPICE simulator. In the computer simulation, the parameter setting of the diode model is as follows: $R_d = 0.1\ \Omega$ and $V_{th} = 0.36$ V, where we assumed a Schottky barrier diode (SBD). To clarify the effectiveness of the proposed converter, the characteristics of the proposed converter are compared with the conventional converters shown in Figures 4-6, namely, SISO Cockcroft-Walton converter (Conv.-1), SISO Dickson converter (Conv.-2), and SISO HCWD converter (Conv.-3).

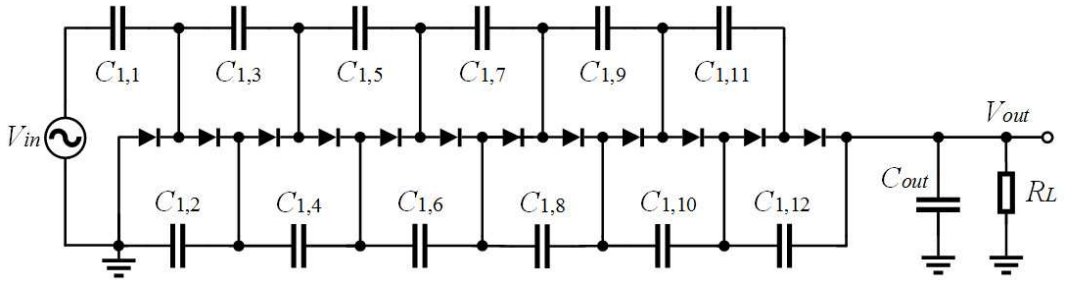


FIGURE 4. Single-input single-output Cockcroft-Walton converter

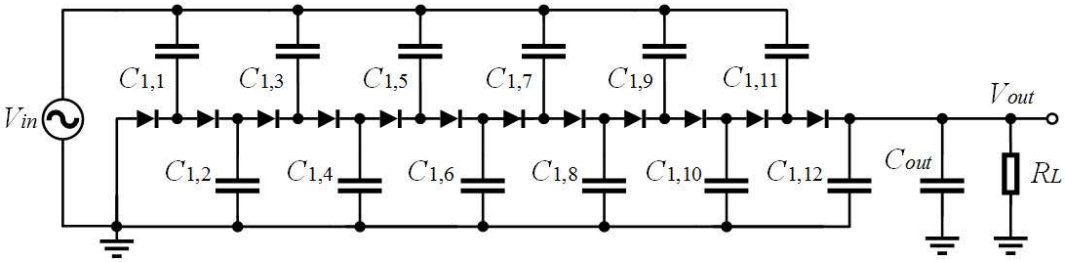


FIGURE 5. Single-input single-output Dickson converter

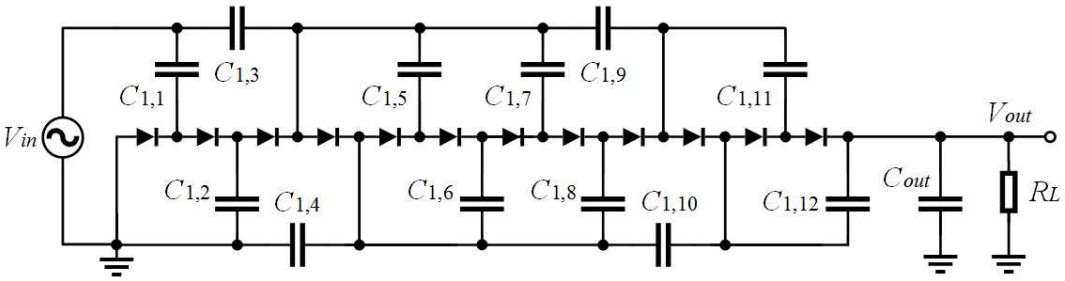
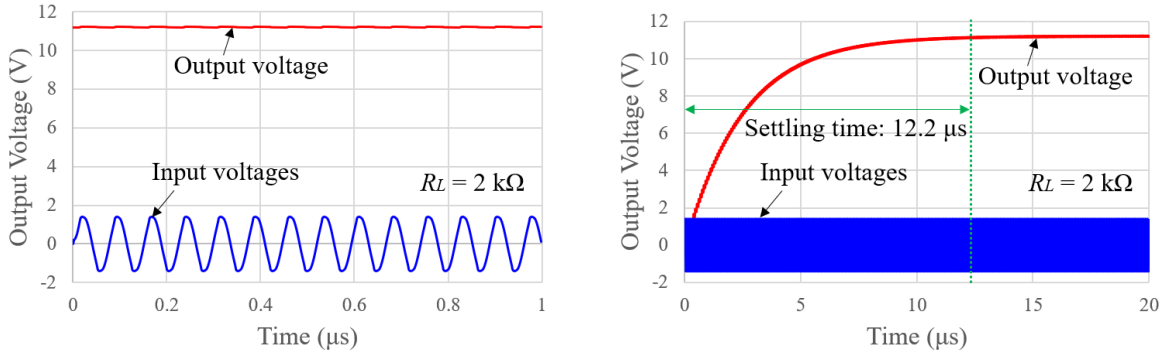


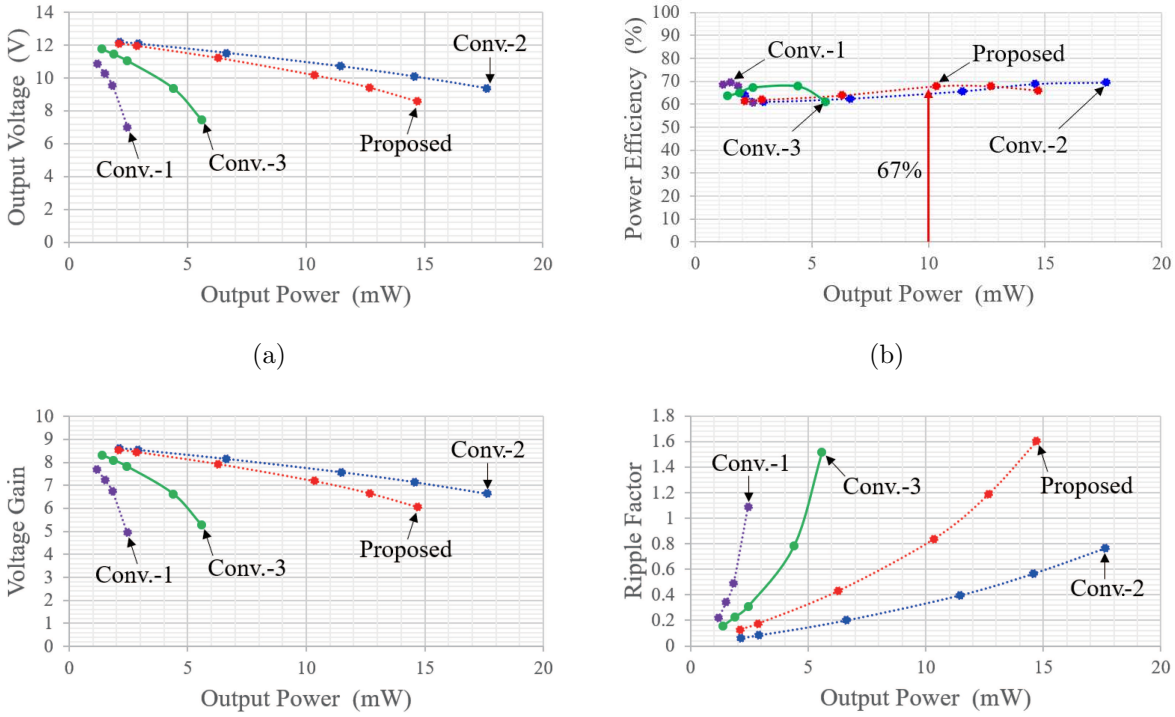
FIGURE 6. Single-input single-output hybrid Cockcroft-Walton/Dickson converter

Figure 7 shows the simulated transient characteristics in steady and transient states when $R_L = 2$ kΩ. As this figure shows, the settling time of the proposed converter is about 12.2 μs. Figure 8 demonstrates the comparison results of the AC/DC converters, where output voltage, power efficiency, voltage gain, and ripple factor were investigated. In these figures, the circuit parameters were set to $V_{in} = V_{in.1} = V_{in.2} = 1$ V at 13.56 MHz, $C_{i,j} = 500$ pF, and $C_{out} = 1$ nF. As these figures show, the proposed converter can provide a DC output by converting the small AC input 1 V at 13.56 MHz. From the simulated result shown in Figure 8(b), the power efficiency of the proposed converter reaches 67% with an output power of 10 mW.



(a) (b)

FIGURE 7. Simulated transient characteristics: (a) Steady state and (b) transient state



(a) (b) (c) (d)

FIGURE 8. Comparison results: (a) Output voltage, (b) power efficiency, (c) voltage gain, and (d) ripple factor

Table 1 describes the feature comparison, where the number of circuit components is the same for all the converters compared. As this table shows, the voltage stress of the proposed converter is the 2nd lowest. Table 2 summarizes the comparison results. It is noteworthy that the proposed converter can achieve the 2nd highest performance on all evaluation criteria. As Table 2 shows, the Conv.-2 shows the best performance in terms of output voltage, power efficiency, voltage gain, and ripple factor. However, due to high voltage stress, it is difficult to apply Conv.-2 to high voltage applications. On the other hand, since the proposed converter has no bottleneck, the application field of the proposed converter is wide.

TABLE 1. Feature comparison

Topology	Voltage stress	Ideal gain	Component count	
			Diode	Capacitor
Proposed	$4\|V_{\max}\|$	12	12	13
Conv.-1	$2\|V_{\max}\|$	12	12	13
Conv.-2	$12\|V_{\max}\|$	12	12	13
Conv.-3	$6\|V_{\max}\|$	12	12	13

TABLE 2. Summary of comparison results

Topology	Output voltage	Power efficiency	Voltage gain	Ripple factor	Voltage stress
Proposed	○	○	○	○	○
Conv.-1	×	×	×	×	◎
Conv.-2	◎	◎	◎	◎	×
Conv.-3	△	△	△	△	△

◎: Excellent, ○: Good, △: Average, ×: Poor

5. **Conclusions.** For 13.56 MHz WPT systems, we have presented a MISO AC/DC converter with HCWD topology in this paper. The theoretical analysis and computer simulations clarified the properties of the proposed converter. The SPICE simulations showed that the proposed converter can provide a DC output from 1 V at 13.56 MHz input, where the power efficiency reached 67% with an output power of 10 mW. Furthermore, as a result of the comparison, it was found that the proposed converter can achieve excellent performance in terms of power efficiency, voltage gain, and ripple factor. From these results, the proposed converter is one of the most promising converters for 13.56 MHz WTP systems. In future research, the feasibility of the proposed converter will be confirmed experimentally.

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