International Journal of Innovative
Computing, Information and Control
Volume **18**, Number **6**, December **2022**

 ISSN 1349-4198
pp. **1979–1988**

DIGITAL FREQUENCY-LOCKED LOOP WITH WIDE LOCK-IN RANGE AND LOW FREQUENCY ERROR BASED ON MULTI-PHASE CLOCK

Mitsutoshi Yahara[1], Kuniaki Fujimoto[2], Daishi Nishiguchi[3]
Yujiro Harada[4] and Masaaki Fukuhara[3]

[1]Department of Medical Care and Welfare Engineering
[2]Department of Electronics and Intelligent Systems Engineering
Tokai University
9-1-1, Toroku, Higashi-ku, Kumamoto-shi, Kumamoto 862-8652, Japan
{ yahara; fujimoto }@tokai.ac.jp

[3]Graduate School of Information and Telecommunication Engineering
Tokai University
2-3-23, Takanawa, Minato-ku, Tokyo 108-8619, Japan
1cjnm012@mail.u-tokai.ac.jp; fukuhara@tokai.ac.jp

[4]Department of Electrical and Electronic Engineering
National Institute of Technology, Kurume College
1-1-1, Komorino, Kurume-shi, Fukuoka 830-8555, Japan
y-harada@kurume-nct.ac.jp

Received June 2022; revised September 2022

Abstract. *An all-digital frequency-locked loop (DFLL) using a multi-phase clock-based $1 + 1/k$ divider has been proposed. This circuit can reduce the jitter of the output signal extremely small. However, it has the problem of a narrow lock-in range. In this paper, we propose a DFLL with a wide frequency lock-in range and low frequency error using the $m + n/k$ divider based on a multi-phase clock. The proposed DFLL can realize an extremely wide frequency lock-in range compared to the conventional DFLL using a multi-phase clock. Also, the frequency detection error between input and output signals can be kept within one phase difference of the multi-phase clock. As a result, the steady-state frequency error of the output signal is also within one phase difference of the multi-phase clock. These characteristics were confirmed by simulation using Verilog-HDL, a hardware description language.*

Keywords: Frequency-locked loop, Multi-phase clock, Frequency error, Divider, PLL

1. **Introduction.** The role of mobile communication devices is becoming extremely important in promoting digital transformation. In that mobile communication device, a clock generator circuit is incorporated for multiple clock distributions to drive various circuits on the system while keeping locked with the microprocessor. Therefore, the accuracy of these clock generation circuits is an extremely important factor in achieving stable operation of the entire system [1-3]. In addition, it is desirable for mobile communication devices to be used for a long time on a single charge. In recent years, the performance of batteries has been improving. However, as the performance of mobile communication devices improves and they are linked with peripheral devices, an increase in power consumption is inevitable. Especially for mobile communication devices that are in standby mode for a long time during use, the power consumption in that state has a significant impact on the power consumption of the entire system. For this reason, it is extremely

DOI: 10.24507/ijicic.18.06.1979

important to stop the clock generation circuit during standby and to supply the clock quickly when it comes back.

A widely used circuit for this clock generation is a phase-locked loop (PLL). However, because PLLs require control of both the phase and frequency between input and output signals, it takes some time to generate a stable clock from the system standby state. To improve this, we can set a shorter time constant for the filter that makes up the loop. However, since the jitter of the output signal increases, there is still a problem in terms of supplying a stable clock [4]. Frequency-locked loops (FLL) and delay-locked loops (DLL) have been proposed as circuits to solve this problem [2,5].

The FLL is a clock generation circuit that only performs frequency lock to the input signal, not phase lock. Hence, compared to PLL, FLL has the advantage of shortening the time required to obtain a stable output signal after the input signal is applied. Also, it is not affected by the clock propagation delay. Furthermore, it can obtain stable operation even if there is a discontinuity in the phase of the input signal. However, in the FLL with analog configuration, it was difficult to configure a frequency comparator to detect the frequency error with fast and accuracy. As a result, there was a difficulty in obtaining an accurately output signal for the frequency of the input signal.

The authors previously proposed the all-digital frequency-locked loop (DFLL) to improve this problem [6-8]. This DFLL can remove the frequency error from the output signal in two cycles of the input signal. Also, it was not affected by the cycle slip between the input and output signals. However, the maximum frequency error between the input and output signals occurred in less than one cycle of the reference clock that controlled the loop. To improve this problem, we proposed a DFLL using multi-phase clocks (hereinafter referred to as conventional DFLL) [9]. The conventional DFLL can reduce the maximum frequency error to less than one phase difference of a multi-phase clock. However, it had the problem of a narrow frequency lock-in range.

In this paper, we propose the DFLL based on a multi-phase clock that can realize both a wide frequency lock-in range and low frequency error. The conventional DFLL was configured to control the frequency of the output signal using a $1+1/k$ divider. In the proposed DFLL, a wide frequency lock-in range can be obtained by using $m+n/k$ divider. Also, since the frequency error control of the input and output signals is controlled by one phase difference unit of the multi-phase clock as in the conventional DFLL, a low frequency error can be realized.

In the following, Chapter 2 describes the basic operation and frequency lock-in range of the conventional DFLL, and Chapter 3 describes the circuit configuration of the proposed DFLL and its operation analysis. Chapter 4 shows the simulation results using Verilog-HDL. Finally, Chapter 5 presents the conclusion.

2. **Frequency Lock-in Range of the Conventional DFLL.**

Figure 1 shows the block diagram of a conventional DFLL. Figure 2 shows the timing chart of the multi-phase clock that controls the loop. Each phase difference of the multi-phase clock should be set to be a fixed interval. The FEC is a counter and control circuit for removing frequency errors between the input and output signals. DC is a digital comparator. The $1+1/k$ is a divider that divides the multi-phase clock by shifting it by one phase. Figure 3 shows the circuit configuration and operating waveforms of the $1+1/k$ divider.

Next, we describe the basic operation of a conventional DFLL. If there is a frequency error between the input signal and the output signal, the frequency comparator based on the multi-phase clock detects the number of phases of the multi-phase clock corresponding to the error as the error value "Q". This frequency error value "Q" is transferred to the FEC. The FEC determines the control value "m" of the $1+1/k$ frequency divider, which

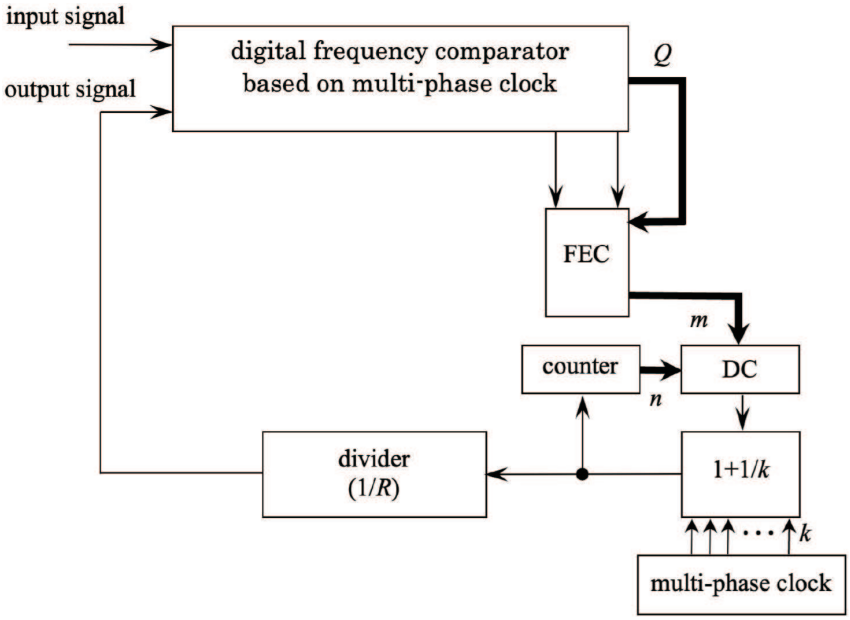

FIGURE 1. Block diagram of the conventional DFLL

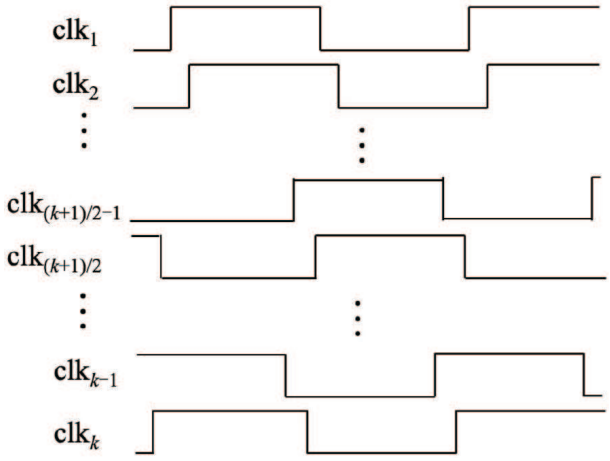

FIGURE 2. Timing chart of multi-phase clock

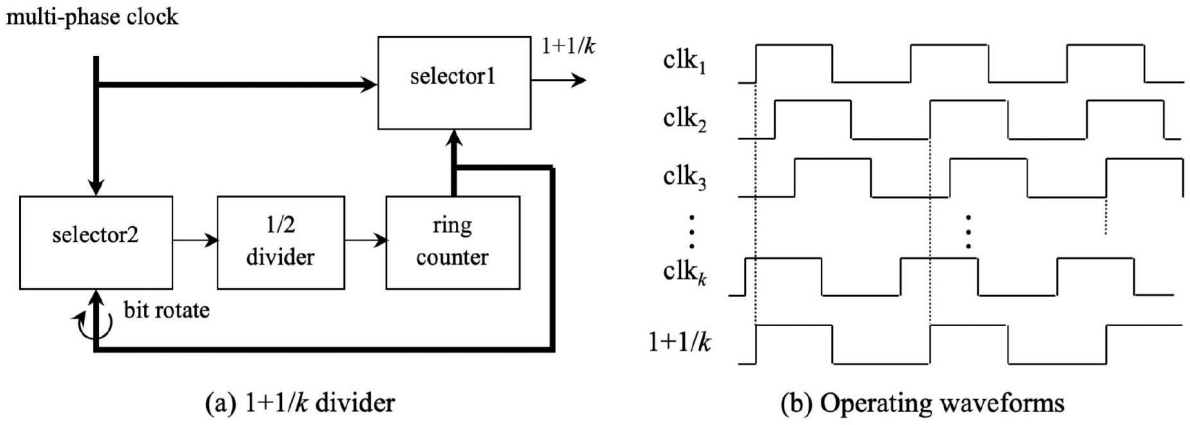

FIGURE 3. Circuit diagram and waveforms of $1+1/k$ divider

is calculated based on the control state before one cycle. The DC compares the value "n" of the counter that counts the number of clocks supplied to the divider with the value "m" from the FEC. While the relationship is "$n \leq m$", the $1+1/k$ divider supplies the divider with a signal that divides the multi-phase clock by $1+1/k$. Also, while "$n > m$", the $1+1/k$ divider does not operate, and the multi-phase clock selected at "$n = m$" is supplied directly to the divider. The divider generates the output signal by dividing these two clocks by $1/R$. Hence, the output signal of the conventional DFLL is a clock generated from "m" multi-phase clocks divided by $1+1/k$ and "$R - m$" multi-phase clocks without division, as shown in Figure 4.

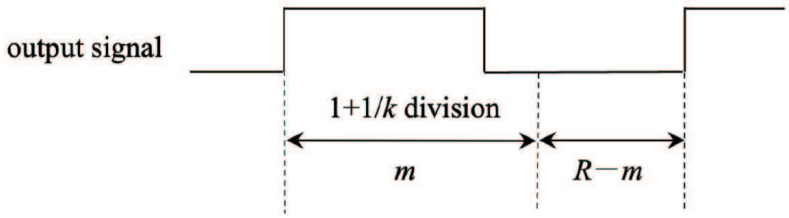

FIGURE 4. Output signal control of the conventional DFLL

From the above operation, the frequency lock-in range of the conventional DFLL is determined by the division ratio "R" and the number "m", which divides the multi-phase clock by $1+1/k$. Since the maximum value of "m" is "R", the lower limit of the division ratio is "R" and the upper limit is "$R(1 + 1/k)$". Therefore, if f_{in} is the frequency of the input signal and f_{mp} is the frequency of the multi-phase clock. The frequency lock-in range of the conventional DFLL is expressed by the following equation.

$$\frac{f_{mp}}{R\left(1+\frac{1}{k}\right)} \leq f_{in} \leq \frac{f_{mp}}{R} \tag{1}$$

3. Circuit Configuration and Operational Analysis of the Proposed DFLL.

3.1. **Circuit configuration of the proposed DFLL.** Figure 5 shows the circuit configuration of the proposed DFLL. This circuit is configured to achieve a wide synchronization range by introducing the $m + n/k$ divider where the $1+1/k$ divider is used for control in the conventional system. Here, T-FF1, T-FF2, T-FF3, EX-OR, logic gate, and U/D-counter_1∼k constitute a digital frequency comparator. U/D-counter_n, U/D-counter_m, and FEC are counters and control circuits for removing frequency errors between input and output signals. The initial value of U/D-counter_1∼k is set to X. The count value "n" of U/D-counter_n is set to the frequency error removal value Q from the FEC. If the relationship between "n" and "x" is "$n > X$", then "n" is down-counted by "k", and at the same time, U/D-counter_m is up-counted by 1. Conversely, if the relationship is "$n < X$", then "n" is up-counted by "k", and at the same time, U/D-counter_m is down-counted by 1. After that, the same operation is repeated until the count value "n" of U/D-counter_n is within the range of "X" to "$X - k$". Figure 6 shows the algorithm of the operation.

3.2. **Circuit configuration and operation of multi-phase clock divider.** Figure 7 shows the circuit configuration of the multi-phase clock divider. DC1 and DC2 are digital comparator. Figure 8 shows the operating waveforms of the multi-phase clock divider. DC1 compares the value "n" of U/D-counter_n with the total value "z" of the counter. While the relationship is "$n > z$", DC1 outputs a low level (from time t_0 to t_1). During this time, the $1+1/k$ divider outputs a signal that divides the multi-phase

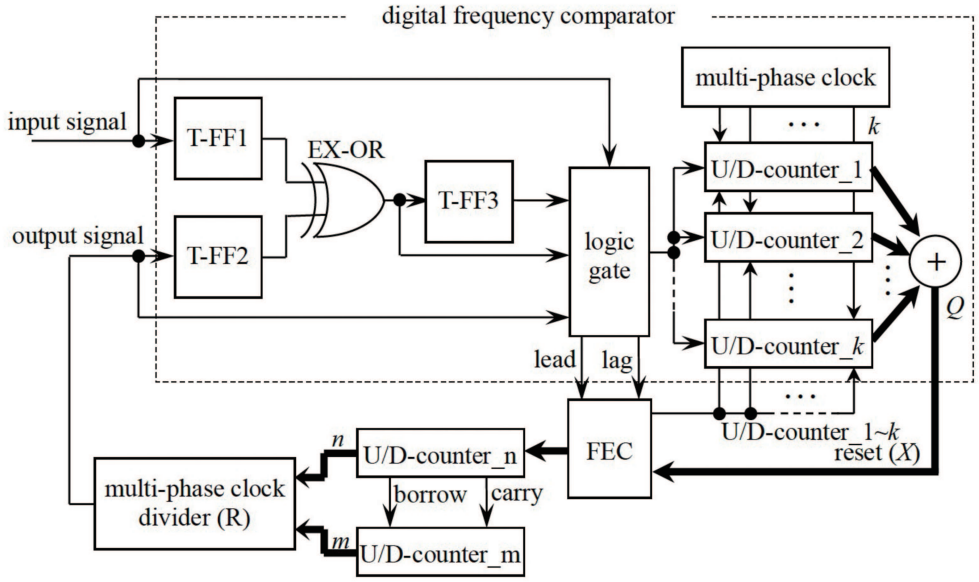

FIGURE 5. Circuit configuration of the proposed DFLL based on double-edge counter

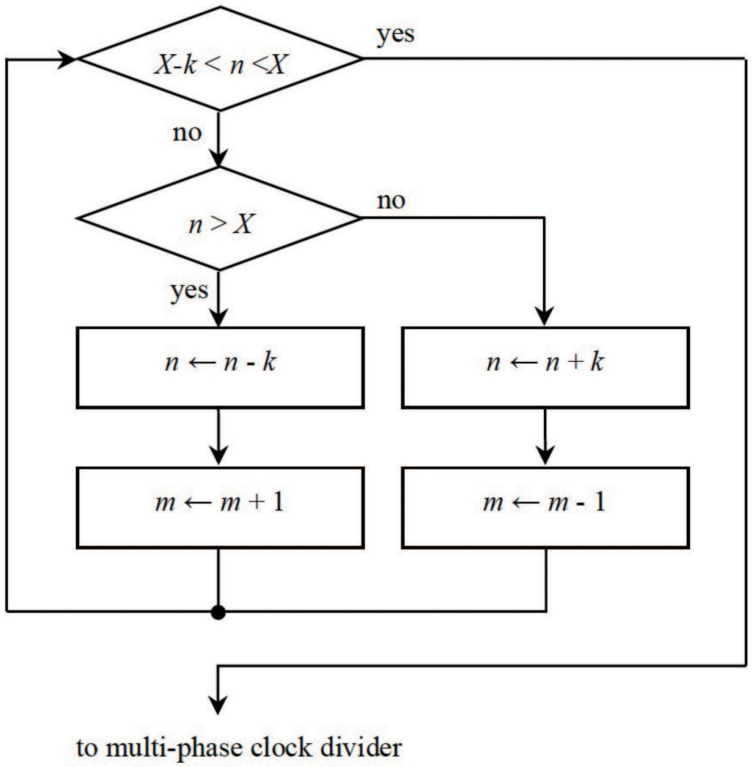

FIGURE 6. Algorithm for each counter operation

clock by $1+1/k$, and the counter counts this signal. At the time t_1, when "z" reaches "n" and the relationship "$n \leq z$", DC1 outputs a high level. Thereafter, the $1+1/k$ divider outputs the multi-phase clock selected at that time without dividing it by $1+1/k$ (time t_1 to t_2). DC2 compares the value "x" of the counter, which counts the signal from the $1+1/k$ divider, with the value "m" of U/D-counter_m, which is the set value of the divider

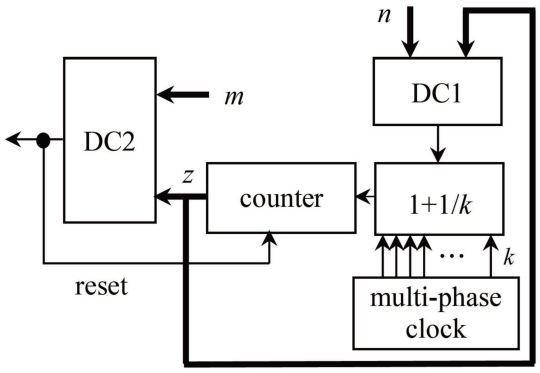

FIGURE 7. Circuit configuration of multi-phase clock divider

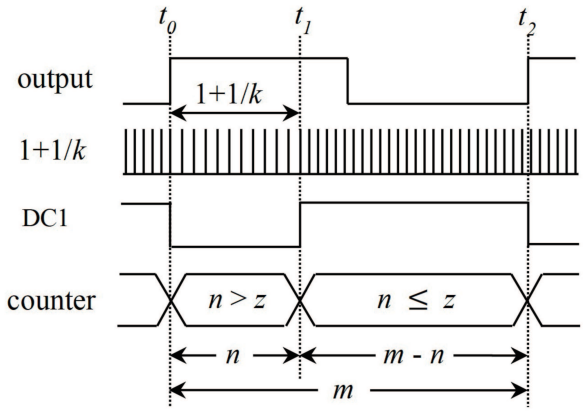

FIGURE 8. Waveforms of multi-phase clock divider

ratio. At the time t_2 when "$z = m$", DC2 outputs a high level, and at the same the time, counter is reset. Therefore, the output signal has "$m - n$" periods of multi-phase clock and "n" periods of the multi-phase clock divided by $1+1/k$ in one cycle. Therefore, if t_{wd} is the time of one phase difference of the multi-phase clock. The time t_{out} of one cycle of the output signal of the proposed DFLL is expressed as

$$t_{out} = (m - n) \cdot t_{wd} + n \cdot t_{wd} \left(1 + \frac{1}{k}\right) = t_{wd} \left(m + \frac{n}{k}\right) \tag{2}$$

If the output frequency of the multi-phase clock divider is f_{out}, the relationship with the multi-phase clock frequency f_{mp} is expressed by the following equation.

$$f_{out} = \frac{f_{mp}}{m + \frac{n}{k}} \tag{3}$$

From this, it is found that the output signal is obtained by dividing the multi-phase clock by $m + n/k$.

3.3. **Operational analysis of the proposed DFLL.** Figure 9 shows the operational waveforms of the proposed DFLL using the multi-phase clock divider. At the time t_1, when the input signal is high, the EX-OR in the digital frequency comparator outputs a high level. Next, when the output signal is high at time t_2, the EX-OR outputs a low level. The output of this EX-OR is divided by T-FF3.

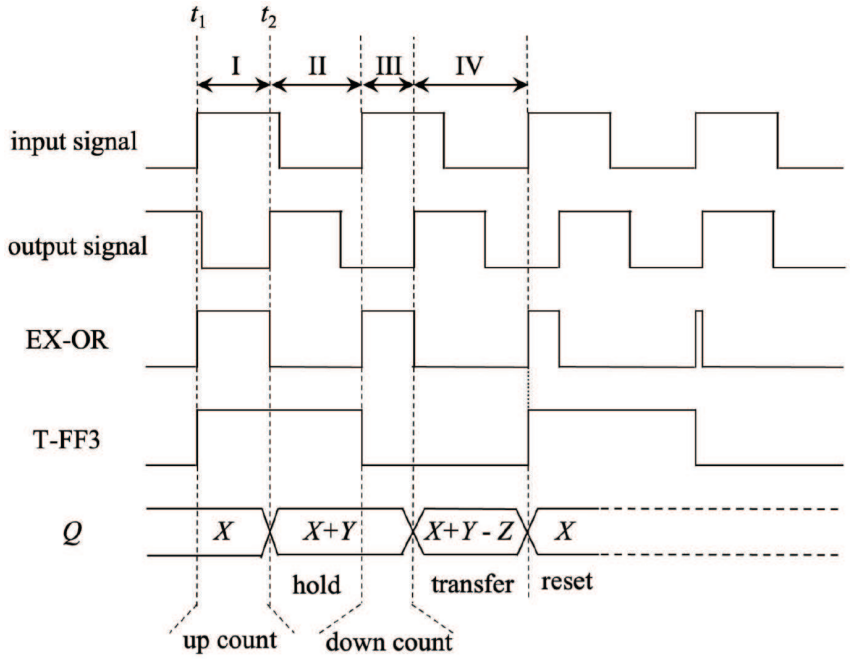

FIGURE 9. Waveforms of the proposed DFLL

Next, we will explain the frequency error detection operation. Now, in state I of Figure 9, the U/D-counter_1∼k up-count each multi-phase clock that passes through from the initial value "X" while the output of EX-OR is high. If the total number of multi-phase clocks that pass through during state I (up-count value) is "Y", the value "Q" of the adder circuit at the end of state I is "$Q = X + Y$".

In state II, the U/D-counter_1∼k and the count value "Q" of the adder circuit are retained.

In state III, the U/D-counter_1∼k down-count the number of each multi-phase clock that passes through while the output of EX-OR is high. If the total number (down count value) of each multi-phase clock that passes during state III is "Z", the value "Q" of the adder circuit is "$Q = X + Y - Z$". As a result, the value "Q" of the adder circuit at the end of state III becomes the value corresponding to the frequency error between input and output signals.

In state IV, the value "Q" of the adder circuit is transferred to the FEC of the next stage. The FEC sets "Q" to U/D-counter_n and down-counts from that value by "k", the number of multi-phase clocks. At the same time, if the up-count value "Y" and the down-count value "Z" of the adder circuit are in the relation "$Y > Z$", the value of U/D-counter_m is down-counted by 1. This operation is repeated until the relation "$n < k$" is reached. If the value of U/D-counter_m before state IV is "m_p", the division ratio "R" at this point is expressed as

$$R = \left(m_p - \left\lfloor \frac{Y - Z}{k} \right\rfloor \right) + \frac{n}{k} \tag{4}$$

From this, the frequency of the output signal will be higher by the difference between "Y" and "Z". As a result, the proposed DFLL operates in the direction of removing the frequency error between the input and output signals.

Conversely, if "Y" and "Z" are in the relationship "$Y < Z$", the value of U/D-counter_m is up-counted. This operation is repeated until the relation "$n > k$" is reached.

At this time, the division ratio "R" is expressed as

$$R = \left(m_p - \left\lfloor \frac{Z - Y}{k} \right\rfloor \right) + \frac{n}{k} \tag{5}$$

As a result, the frequency of the output signal of the proposed DFLL is lowered by the difference between "Y" and "Z", and the same operation is performed. Also, at this point, the count values of U/D-counter_1$\sim k$ are reset to the initial value "X" to prepare for the next count.

Here, we consider the frequency lock-in range and steady-state frequency error of the proposed DFLL. The proposed DFLL is a configuration in which the frequency of the output signal is determined by dividing the multi-phase clock by the division ratio "R". Hence, the range of frequency lock-in is determined by the setting range of the division ratio "R". If the lower and upper limits of the division ratio "m" are "$m_{\min}$" and "$m_{\max}$", respectively, the frequency lock-in range of the proposed DFLL is expressed by the following equation.

$$\frac{f_{mp}}{m_{\max} + \frac{k-1}{k}} \leq f_{in} \leq \frac{f_{mp}}{m_{\min}} \tag{6}$$

Next, we consider the steady-state frequency error. The multi-phase clock and the input signal of the proposed DFLL are not locked. Also, since the frequency control of the output signal is in units of one phase difference of the multi-phase clock, the output signal has a maximum steady-state frequency error of that one phase difference. Therefore, the average frequency f_{avg} of the output signal is expressed by the following equation.

$$f_{avg} = \frac{\frac{f_{mp}}{\left(m + \frac{n}{k}\right)} + \frac{f_{mp}}{\left(m + \frac{n}{k}\right) \pm \frac{1}{k}}}{2} \tag{7}$$

From this, if the frequency division ratio "m" is set somewhat large in the proposed FLL, the effect of this error on the jitter suppression effect can be ignored.

4. **Simulation Result.** The simulation was performed using Verilog-HDL, a hardware description language.

Table 1 shows the frequency lock-in ranges of the proposed DFLL and the conventional DFLL. In this simulation, from the viewpoint of comparing the lock-in range of the proposed DFLL and the conventional DFLL, the lower limit of the division ratio is set to $m_{\min} = R = 50$ so that the upper frequency limit of the lock-in range is the same, according to Equations (1) and (6). From this, it is found that the lock-in range of the proposed DFLL is extremely wide compared to the conventional DFLL. Also, the range satisfies Equation (6), and can be adjusted according to the intended and output jitter characteristics use by $m_{\max}$ and $m_{\min}$.

TABLE 1. Frequency locked range

	$f_{mp} = 2\text{MHz}$, $k = 7$, $m_{\max} = 100$
Conventional DFLL	35kHz $\sim$ 40kHz
Proposed DFLL	19.8kHz $\sim$ 40kHz

Figure 10 shows the simulated waveforms of each part of the proposed DFLL. The proposed DFLL performs the counting operation within one phase difference of the multi-phase clock after the frequency error signal rises or before it falls. Hence, it is found that the frequency detection error is controlled within one phase difference of the multi-phase clock.

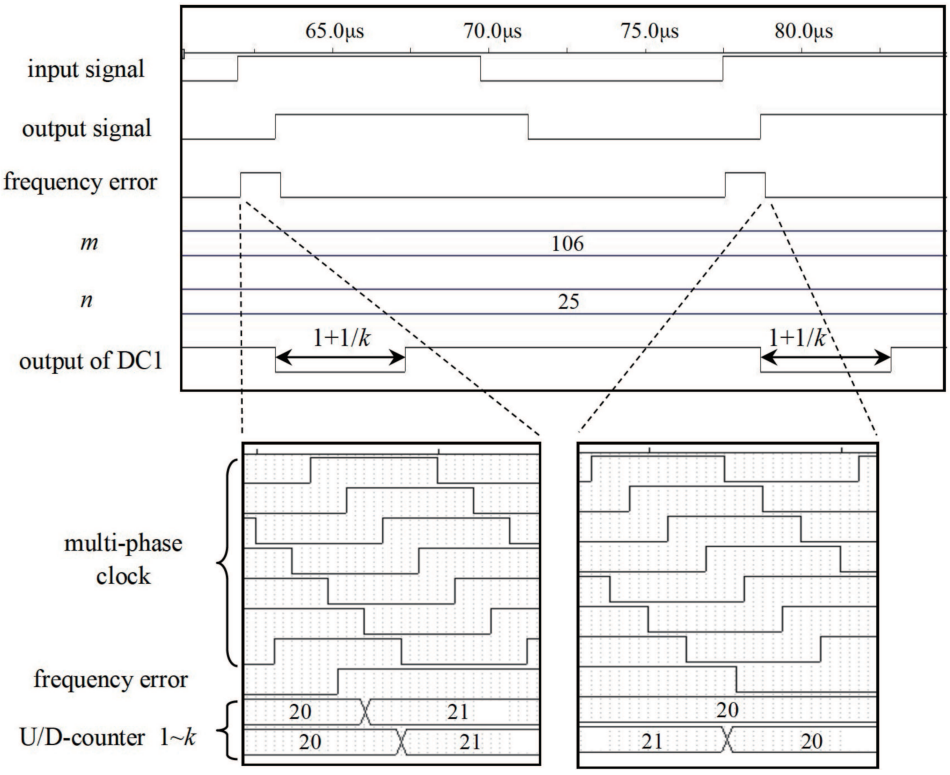

FIGURE 10. Simulation waveforms of the proposed DFLL

5. **Conclusion.** In this paper, we proposed a DFLL that can realize both a wide frequency lock-in range and a low frequency error by using the $m+n/k$ divider based on the multi-phase clock. The proposed DFLL can obtain an extremely wide frequency lock-in range compared to the conventional DFLL. Also, this range can be adjusted according to the set value of the division ratio "m". Also, this range can be adjusted according to the intended use by setting the division ratio "m". Furthermore, since the frequency error control between input and output signals is controlled by one phase difference unit of the multi-phase clock, the steady-state frequency error can be kept within its range.

In the future, we plan to further verify the characteristics and study its practicality.

REFERENCES

[1] Y. Harada, M. Yahara, K. Eguchi and K. Fujimoto, A flash type A/D converter using neuron CMOS inverters with threshold compensation circuits, *ICIC Express Letters*, vol.14, no.3, pp.251-256, 2020.

[2] M. Miyazaki and K. Ishibashi, A 3-cycle lock time delay-locked loop with a parallel detector as a low-power system-clock generator, *IEICE Trans. Electronics*, vol.J83-C, no.6, pp.502-508, 2000.

[3] K. Eguchi, A. Shibata, T. Ishibashi and I. Oota, An inductor-less nesting-type step-up/step-down AC/AC converter with a small component count, *International Journal of Innovative Computing, Information and Control*, vol.15, no.6, pp.2377-2384, 2019.

[4] M. Yahara, K. Fujimoto and H. Kiyota, Multiple frequency digital phase-locked loop based on multi-phase clock divider with constant pulse interval, *IEEJ Trans. Electronics, Information and Systems*, vol.138, no.4, pp.387-394, 2018.

[5] K. Tanaka, A. Hyogo and K. Sekine, A frequency synthesizer using a frequency locked loop, *IEICE CAS89-64*, pp.73-78, 1989.

[6] M. Yahara, K. Fujimoto, Y. Harada and K. Matsumoto, A 2-mode digital FLL using frequency comparator corresponding to cycle slip, *ICIC Express Letters, Part B: Applications*, vol.8, no.9, pp.1271-1278, 2017.

[7] M. Yahara, K. Fujimoto and D. Nishiguchi, A reset type 2-mode digital FLL with anti-pseudo-lock function and phase control, *ICIC Express Letters, Part B: Applications*, vol.10, no.10, pp.903-910, 2019.
[8] M. Yahara, K. Fujimoto, D. Nishiguchi and Y. Harada, Digital frequency-locked loop based on double-edge counter, *ICIC Express Letters, Part B: Applications*, vol.12, no.5, pp.427-434, 2021.
[9] M. Yahara, K. Fujimoto, D. Nishiguchi, Y. Harada and M. Fukuhara, Digital frequency-locked loop with low frequency error based on multi-phase clock, *ICIC Express Letters*, vol.16, no.2, pp.159-167, 2022.

Author Biography

Mitsutoshi Yahara graduated from Kyushu Tokai University (Dept. of Eng.) in 1991, where he completed master's course in 1993. He was employed as an assistant by Tokai University Fukuoka Junior College where he was a lecturer in 1997, was a professor in 2009, and has been a professor at Tokai University since 2018. He obtained his Ph.D. in Engineering from Tokai University in 2007. His research interests include switched capacitor circuits and phase-locked loops.

Kuniaki Fujimoto graduated from Tokai University (Dept. of Eng.) in 1987, where he completed master's course in 1989, and was employed as an assistant by Nagasaki Women's Junior College. He was an assistant at Kyushu Tokai University in 1991, and has been a professor at Tokai University since 2010. He obtained his Ph.D. in Engineering from Tokai University in 2009. His research interests include pulsed circuits and digital circuits.

Daishi Nishiguchi graduated from School of Industrial and Welfare Engineering, Tokai University in 2021. He entered Graduate School of Tokai University in the same year, and is currently studying there. He engages in studies related to electronic neuron circuit and digital circuit.

Yujiro Harada obtained his Ph.D. in Engineering from Tokai University in 2017. He is currently a full-time assistant professor at the National Institute of Technology, Kurume College, Japan. His main research interests include the A/D converter and the associative memory.

Masaaki Fukuhara received the B.S. degree in Telecommunication Engineering, the M.S. and the Ph.D. degrees in Electrical Engineering from Tokai University, Japan, in 2002, 2004, and 2007, respectively. He has been a lecturer and an associate professor at the School of Information and Telecommunication, Tokai University Takanawa campus since 2013 and 2019, respectively. His main interest is in the application area of neuron MOS technology to improve any electronic and integrated circuit, including CAM (Content Addressable Memory) and FPGA (Field Programmable Gate Array).