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IMPLEMENTATION OF SOGI-PLL ALGORITHM FOR SINGLE PHASE GRID CONNECTED INVERTERS BASED ON FIXED-POINT ARITHMETIC

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Abstract. *The tracking performance of a phase-locked loop (PLL) algorithm in grid-connected power electronic systems significantly contributes to the success of grid synchronization. This paper presents an efficient software realization of SOGI-PLL (second order generalized integrator – phase locked loop), as one of the most popular single-phase grid synchronization strategies in practice. The utilization of floating-point processors has been relatively common; however in this work, the SOGI-PLL is implemented using the fixed-point arithmetic technique in consideration of delivering a low-cost and compact hardware solution. Fixed-point microcontrollers or DSPs are still widely used by many researchers, developers, and practical engineers due to their cost-efficient implementation in both hardware and development software tools. In this work, the implementation of the SOGI-PLL algorithm in fixed-point arithmetic is demonstrated using C programming in a low-cost 16-bit fixed-point DSC dsPIC30F3014 with a 20 MHz crystal clock. Based on the implementation results, the developed SOGI-PLL algorithm can accurately estimate the grid's fundamental voltage parameters such as the voltage magnitude, phase angle, and frequency.*

Keywords: Fixed-point arithmetic, Grid-connected inverter, SOGI-PLL, Single-phase grid, Synchronization

1. **Introduction.** Nowadays grid-tied inverters have played an important role in various electrical power system applications. The successful operations of the grid-tied inverters rely on a key component known as a phase-locked loop (PLL), which is responsible for estimating grid voltage parameters such as the magnitude of voltage, frequency, and phase angle. This information of the grid parameters is basically essential to synchronize the operation of grid-connected devices with the grid. Several grid-tied inverter applications include grid-connected renewable energy generation systems [1-4], active power filters [5,6], dynamic voltage restores – DVR [7,8], and active rectifiers [9]. In addition, the estimation accuracy of the PLL algorithm is highly dependent on the quality of the power

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grid voltage; therefore, the use of advanced PWM drive methods in grid-tied inverter control system such as selective harmonic elimination (SHE) strategy [10] or others is very important.

For single-phase grid-tied inverter applications, several synchronization methods have been proposed in pieces of literature with their pros and cons. One of the simplest synchronization methods is a zero-crossing detector or ZCD [11]. The ZCD basically is a comparator used to detect the transition of the grid sinusoidal waveform from positive to negative cycles or vice versa. Although the strategy is relatively robust to variation of the grid frequency, this strategy detects zero-crossing point only at every half period of the voltage waveform, so the dynamic performance of the strategy is less sufficient and prone to voltage variations such as sags, notches, and harmonics [12].

Besides the zero-crossing detector, the other single-phase grid synchronization methods or grid parameter estimators proposed by literature include inverse park transform-PLL, enhanced-PLL, complex coefficient filters – PLL, transport-delay-based phase-locked loop, etc. [13,14]. The estimator structures proposed in this literature basically aim to improve the accuracy of the parameters of the electric grid against the influence of network pollution or the imperfection of the voltage sensor used in the application. However, from the popular point of view due to its simplicity of structure and ease of realization, there are at least two methods that are adopted in most applications: T/4 delay PLL [15] and second order generalized integrator – SOGI-PLL [16,17].

The main difference between the above two PLL methods is in how the systems generate an orthogonal signal (a signal that has a 90° phase difference from the original single-phase signal). In the T/4 delay-PLL, the orthogonal signal from the 50 Hz input is achieved by delaying 0.005 seconds (1/4 period) of the input waveform. In the digital implementation with a sampling frequency fs = 10 kHz, the orthogonal signal is obtained by delaying signal acquisition by 50 samples. As far as the grid voltage signal frequency is very close to the nominal value, the estimation results will be accurate. The main disadvantage of this method is the degrading accuracy for relatively large grid frequency deviations. It is also less efficient to be implemented by software due to the requirement of cascaded 50-unit delays [18].

Differing from the T/4 delay PLL method, the orthogonal signal in the SOGI-PLL is generated through a second order generalized integrator filter. To obtain the best performance, the parameters of the filter should be tuned such that it just passes frequencies near the nominal fundamental one. From the software realization point of view, this filter is far more efficient than the T/4 delay method.

Although there have been several pieces of literature concerning the SOGI-PLL implementation on digital machines, to the best of our knowledge, the implementation of the SOGI-PLL algorithm in many pieces of literature is usually realized using floating point arithmetic computation, either developed directly using C or even using a high-level tool such as Simulink coder (with certain hardware platform – such as the evaluation board dSPACE1006 controller).

To get a low-cost and compact hardware solution for the grid-connected device control systems, it is necessary that the PLL algorithm could be implemented at a low-cost single processor unit along with other software components (such as input signal filters, current controller, and DC bus voltage regulator). In considering those reasons, the realization of the PLL by using a fixed-point arithmetic technique which is computationally efficient is urged.

The main objective of this paper is to present a practical implementation of the SOGI-PLL by using the fixed-point arithmetic technique. Some practical issues related to fixed-point arithmetic usage, namely fixed-point format conversion and overflow/underflow

handling are also discussed. Although the utilization of fixed-point arithmetic practically requires special treatment than the floating point one, the machine codes generated by this technique are computationally fast and efficient. In this work, the developed PLL algorithm was embedded in a low-cost 16-bit fixed-point processor dsPIC30f4011 digital signal controller from Microchip and is executed every 0.1 milliseconds.

The rest of this paper is organized as follows. In Section 2, the model of SOGI-PLL both in continuous and discrete models is discussed first. In Section 3, the fixed-point arithmetic implementation model of the SOGI-PLL algorithm is given. Whereas the results of the implementation and conclusion respectively will be presented in Sections 4 and 5.

2. **Linearized SOGI-PLL Model.** Based on its operation principle, the SOGI-PLL could be decomposed into four main functional blocks: 1) a second order generalized integrator-based orthogonal signal generator – SOGI OSG, 2) a park transform, 3) a low pass filter, and 4) an integrator. The interconnection between the blocks is shown in Figure 1. In this case v_a, v_α, and v_β respectively are the grid voltage input, SOGI OSG direct output and orthogonal output, v_d and v_q respectively are well known as the direct and quadrature signals, whereas ω_0, $\Delta\hat{\omega}$, $\hat{\omega}$, and $\hat{\theta}$ are the nominal grid frequency, frequency deviation, estimated frequency and estimated phase angle, respectively.

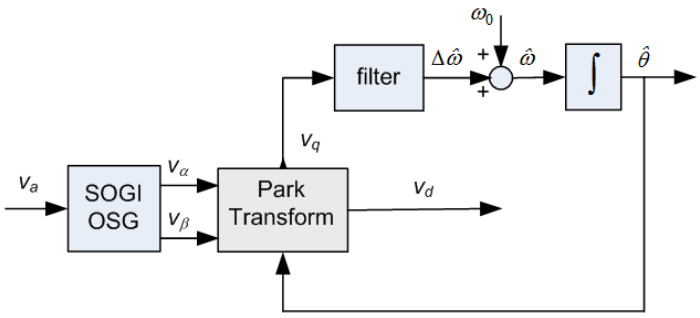


FIGURE 1. Block diagram of SOGI-PLL

The SOGI OSG is basically a second-order filter that passes the input signal and its orthogonal signal at a certain desirable frequency (ω_0). Figure 2 shows a general block diagram of the SOGI OSG. From control system point of view, the SOGI-PLL could be regarded as a feedback control system with its transient characteristic determined by a gain proportional K.

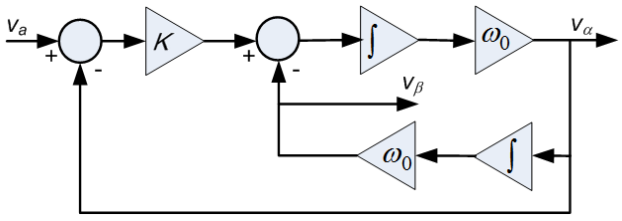
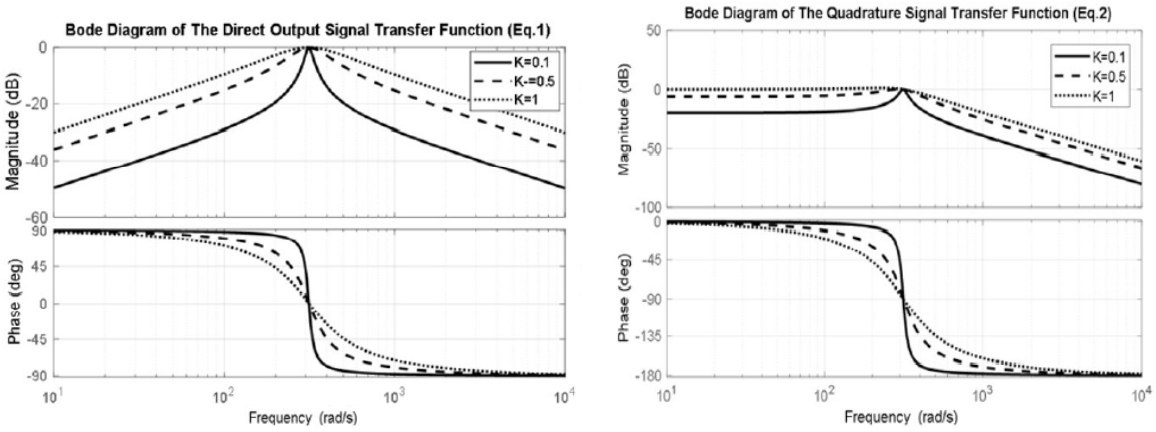


FIGURE 2. Block diagram of the SOGI OSG continuous model

By referring to the signal flow in Figure 2, the relation between the SOGI OSG direct output signal and the orthogonal signal to the input signal in the Laplace domain could be represented respectively by (1) and (2). Figure 3 shows their frequency characteristic for several values of the proportional gains (K).

$$\frac{v_\alpha}{v_a} = \frac{K\omega_0 s}{s^2 + K\omega_0 s + \omega_0^2} \tag{1}$$

$$\frac{v_\beta}{v_a} = \frac{K\omega_0^2}{s^2 + K\omega_0 s + \omega_0^2} \tag{2}$$



(a) (b)

FIGURE 3. Bode diagram of v_α (a) and v_β (b) for several values of K

Based on Figure 3, it can be seen that the SOGI-PLL is basically a band pass filter that passes the power grid signal with a frequency of ω_0. From Figure 3(a) and Figure 3(b) respectively it is clear that, the phase of the output signal v_α will be the same as the phase of input signal while the phase of the output signal v_β will have a phase delay of 90 degrees with respect to the input signal.

From the plots it can also be seen that the proportional gain K which is chosen will greatly determine the bandwidth of the system. The larger the K value, then the frequency band will tend to be wider that makes the system more responsive. However, by using the bigger K, the system will have less relative stability. To obtain the optimal gain K, one should compromise between transient and steady state stability.

If the SOGI OSG input signal is represented by (3), then the SOGI OSG direct output signal and orthogonal signal in the steady state respectively could be represented by (4) and (5).

$$v_a = v_m \cos(\theta) \tag{3}$$

$$v_\alpha \approx v_a = v_m \cos(\theta) \tag{4}$$

$$v_\beta = v_m \sin(\theta) \tag{5}$$

Then by using Park transform (6), the direct (v_d) and quadrature (v_q) signals are obtained.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{6}$$

Substituting (4) and (5) to (6) and doing simplification, the output of Park transform then could be represented by (7) [19].

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} v_m \cos\left(\theta - \hat{\theta}\right) \\ v_m \sin\left(\theta - \hat{\theta}\right) \end{bmatrix} \tag{7}$$

By considering the fact that $\theta - \hat{\theta}$ practically is a very small number, then (7) could be more simplified as seen in (8)

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} \approx \begin{bmatrix} v_m \\ v_m\left(\theta - \hat{\theta}\right) \end{bmatrix} \tag{8}$$

From (8), one can see that the direct (v_d) and quadrature (v_q) components of the voltage vector respectively have a direct relation with the magnitude of the grid voltage input and the phase estimation error. By considering $\theta = \theta_0 + \Delta\theta$ and $\hat{\theta} = \theta_0 + \Delta\hat{\theta}$, then (8) could be rewritten as shown in (9).

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} \approx \begin{bmatrix} v_m \\ v_m\left(\Delta\theta - \Delta\hat{\theta}\right) \end{bmatrix} \tag{9}$$

Therefore, by referring to the last equation, the block diagram of the SOGI-PLL in Figure 1 could be represented in the form of a linear system as depicted in Figure 4.

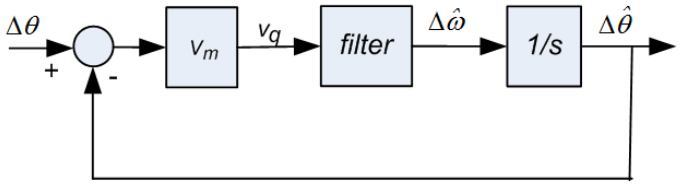


FIGURE 4. Block diagram of the linearized SOGI-PLL

If one chooses the proportional integral PI component (10) as the filter of the SOGI-PLL, then the feedback loop transfer function of the PLL could be represented by (11). In this case, K_p and K_i respectively are a proportional and an integral gain, whereas ω_n and ξ respectively are a natural frequency and damping ratio of the feedback system. For a certain expected ω_n and ξ, the feedback gains could be obtained by using relations (12) and (13).

$$H_{PI}(s) = K_p + K_i\frac{1}{s} \tag{10}$$

$$H_{PLL}(s) = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{11}$$

where

$$\omega_n = \sqrt{K_i v_m} \tag{12}$$

$$\xi = \frac{K_p v_m}{2\sqrt{K_i v_m}} \tag{13}$$

By utilizing a simple backward difference method with sampling time T_s, the discrete mathematical model of the SOGI OSG could be represented by (14) to (16) [20]. Whereas the discrete mathematical model of the PI filter and the integrator could be represented by (17), (18) and (19), respectively.

$$e[k] = v_\alpha[k] - v_\alpha[k-1] \tag{14}$$

$$v_\alpha[k] = v_\alpha[k-1] + \omega_0 T_s(K_p e[k] - v_\beta[k-1]) \tag{15}$$

$$v_\beta[k] = v_\beta[k-1] + \omega_0 T_s v_\alpha[k] \tag{16}$$

$$\Delta\hat{\omega}_i[k] = \Delta\hat{\omega}_i[k-1] + K_i T_s v_q[k] \tag{17}$$

$$\Delta\hat{\omega}[k] = \Delta\hat{\omega}_i[k] + K_p v_q[k] \tag{18}$$

$$\hat{\theta}[k] = \hat{\theta}[k-1] + T_s\left(\Delta\hat{\omega}[k] + \omega_0\right) \tag{19}$$

3. **Design and Implementation of SOGI-PLL by Using Fixed-Point Arithmetic.** In this work, the SOGI-PLL algorithm is developed using C programming language and embedded in the low-cost 16-bit DSC dsPIC30f4011 with just 20 MHz crystal oscillator. Since this DSC has no internal DAC, then to observe the internal variables, we utilize the external dual channel 8-bit DAC AD7302. Figure 5 shows the prototype of the grid-tied inverter system in our laboratory to test the developed SOGI-PLL algorithm.

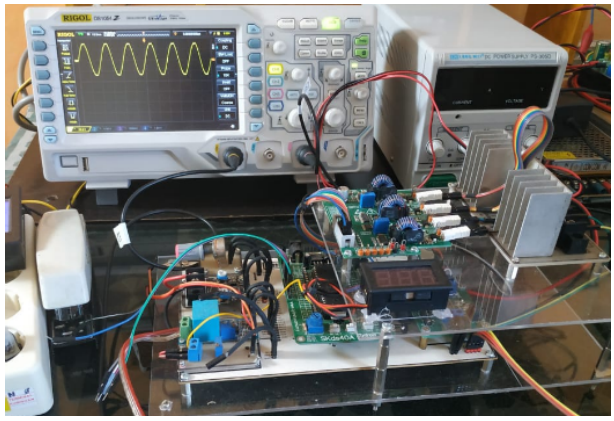


FIGURE 5. The prototype of the grid-tied inverter system

To speed up the execution time, the sine and cosine functions which have high computational demand are precalculated and stored in the 8-bit width look up table with Q1.15 data format (see Figure 6).

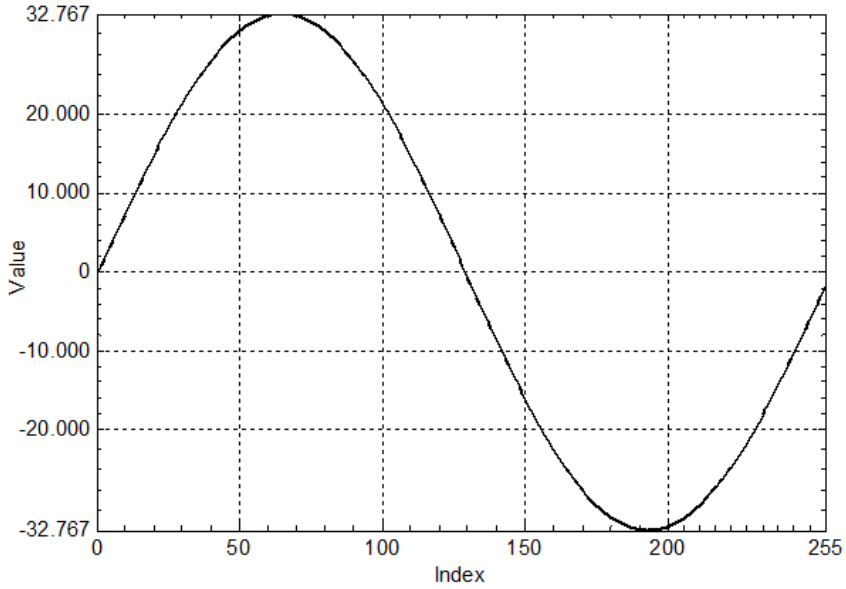


FIGURE 6. Precalculated sin(.) and cos(.) function that is stored in 8-bit width look up table

The main physical quantities, such as the grid voltage, frequency, phase, are represented by using pu variables (fixed-point numbers) and manipulated by fixed-point arithmetic. Table 1 shows the maximum value of the program variables. As shown in Table 1, the maximum value of the grid voltage magnitude and its estimation variable, in this case, is set at 350 V, while the maximum value of the grid frequency and its deviation is set at 51

TABLE 1. SOGI-PLL variables with their max. value

Variables	Max. physical value (base)
v_a, v_α, v_β, v_d, v_q	350 volt
$\Delta\hat{\omega}$	320.28 rad/s
$\hat{\omega}$	320.28 rad/s
$\hat{\theta}$	6.28 rad
sin(.), cos(.)	1

Hz or 320.28 rad/s, while the maximum value of the voltage phase angle and the output of the sinusoidal function is 360° (6.28 rad) and 1, respectively.

In this application program, the proportional and integral gains are set at 1 (0.9999) and 5, respectively, while the nominal grid voltage frequency on the SOGI-PLL is 50 Hz (314 rad/s). Table 2 shows the values of these constants along with other constants required by the application program based on Equations (14)-(19). While the Bode diagram of the SOGI-PLL with these parameters is shown in Figure 7.

Because the real-time SOGI-PLL program acquires the physical quantity-grid voltage via 10-bit ADC, the format of the ADC data output should be converted first to the

TABLE 2. Constants

Program constants	Physical value	pu value	(Q1.15)
ω_0	314 rad/s	0.98	32111
T_s	0.0001 s	0.0001	3
K_p	0.9999	0.9999	32763
$\omega_0 T_s$	0.0314	0.0314	1028
$K_i T_s$	0.0005	0.0005	16

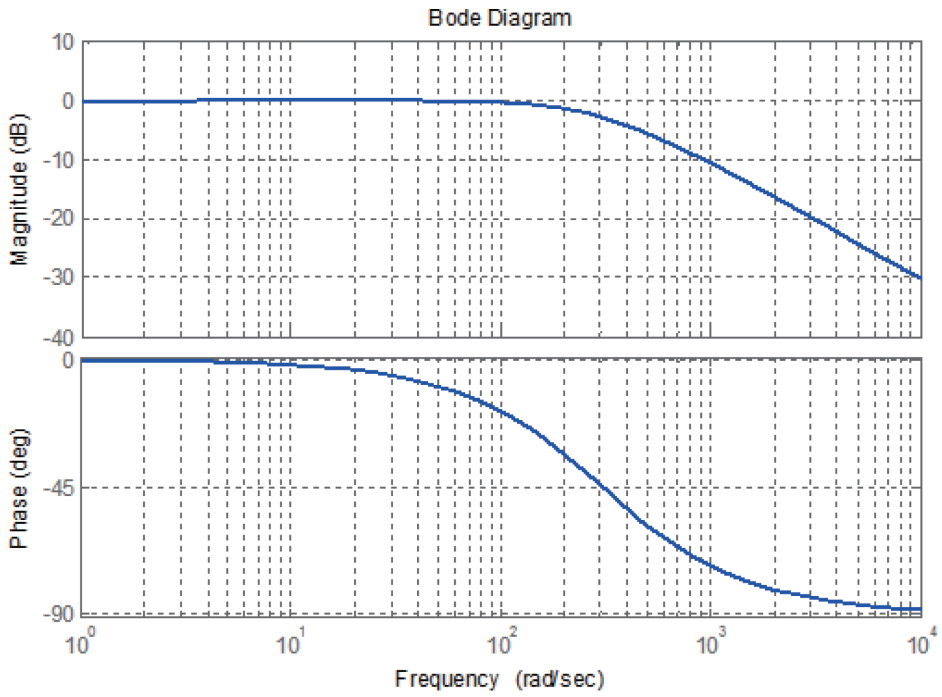


FIGURE 7. Bode diagram of the $\Delta\hat{\theta}$ for $K_p = 1$ and $K_i = 5$

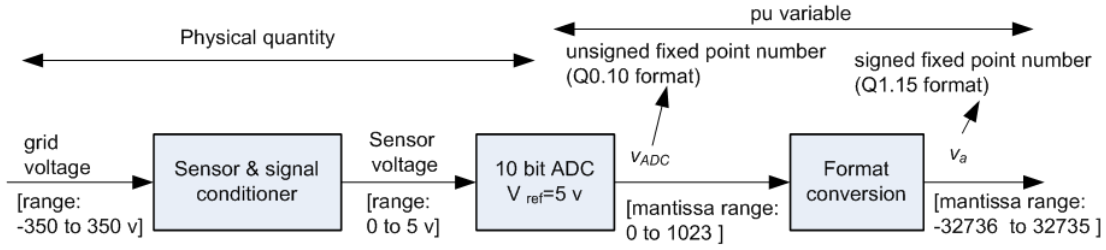


FIGURE 8. Block diagram of the pre-processing steps

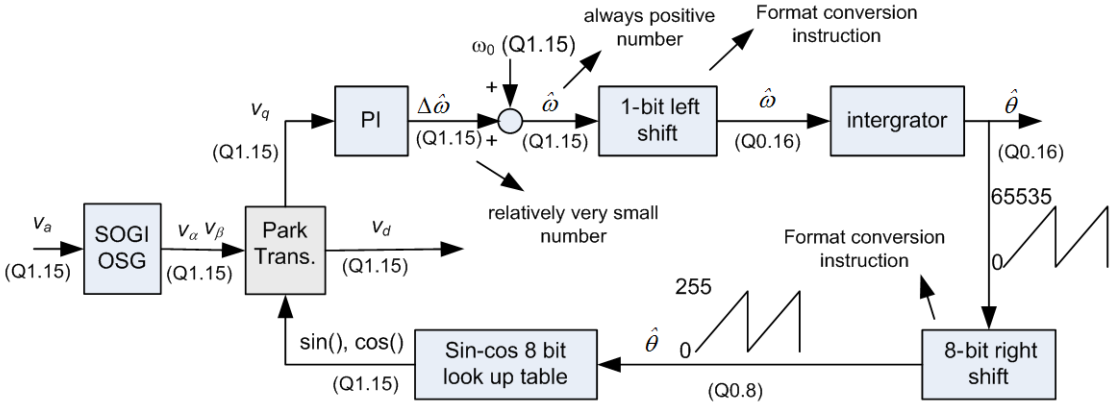


FIGURE 9. Fixed-point arithmetic data flow model of the developed SOGI-PLL algorithm

appropriate format Q1.15. This format conversion process is shown in Figure 8, whereas the main data flow model of the developed SOGI-PLL algorithm is depicted in Figure 9.

Based on Figure 9, it can be seen that the estimation process of the phase angle, frequency and magnitude of the grid voltage starts from filtering the grid voltage signal by the SOGI OSG to produce an estimated voltage signal and its orthogonal signals (v_α and v_β), and the two sinusoidal signals are then transformed into DC signals by Park transform where the estimated phase angle is obtained from the output of feedback control system. As shown in the figure, the output of the Park transform v_q signal is fed back to a proportional integral (PI) filter system to force that signal to be equal to zero. If the v_q signal is being zero, it means that the observer's reference frame is aligned with the original signal, so in this case, the estimated phase angle is the same as the original signal. To accelerate computation time, from Figure 9 it can also be seen that the calculation of the sinusoidal function in this implementation is realized by the look up table technique.

4. **Simulation and Experiment Result.** In this section, the simulation model and real-time SOGI-PLL implementation results are delivered. The model parameters used for both two models are the same as represented in Tables 1 and 2.

Figures 10 to 12 show simulation results of the SOGI-PLL model that runs under Simulink MATLAB simulation software. For grid voltage input (in pu) given in Figure 10(a), the direct output and quadrature signal response of the SOGI OSG block is shown in Figure 10(b). As a comparison, Figure 10(c) shows the results of the orthogonal signal estimation of the SOGI OSG vs quarter delay OSG output. Based on the plots, it appears that in a transient state, the output response of the SOGI OSG is relatively fast compared to the estimated results of the quarter delay OSG.

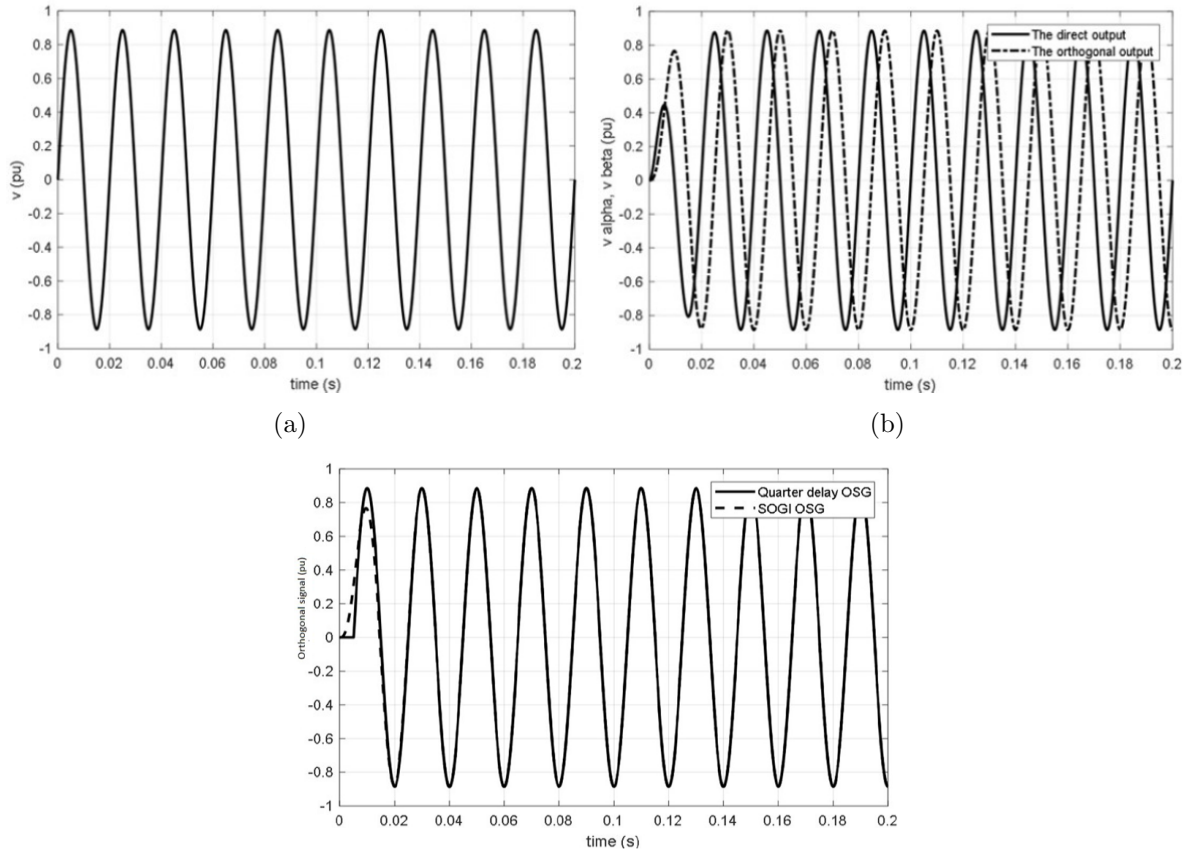


FIGURE 10. Simulation result: (a) Grid voltage input with peak 310 volt (0.8 pu); (b) output of SOGI OSG direct output and orthogonal output; (c) orthogonal signal estimation of the SOGI OSG vs quarter delay OSG output

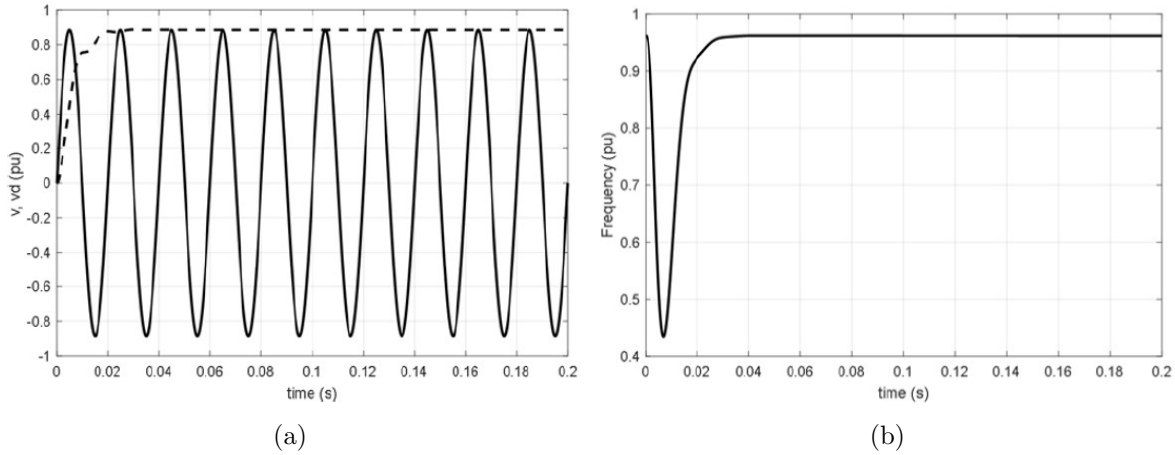


FIGURE 11. Simulation result: (a) Estimated magnitude voltage (dash line), grid voltage (solid line); (b) estimated grid voltage frequency

Figure 11(a) and Figure 11(b) respectively show the estimated grid voltage magnitude (along with the grid voltage input) and estimated frequency of the SOGI-PLL.

As shown at these plots one can see that the SOGI-PLL model could estimate the grid voltage magnitude and frequency accurately in about 20 ms. Whereas the estimated phase angle from the SOGI-PLL is shown in Figure 12 along with the grid input signal. From that plot, one can see that the SOGI-PLL model could estimate phase angle of the grid input signal accurately and quickly. It needs about 21 ms in transient state such that the algorithm model could estimate the true phase angle of the input signal.

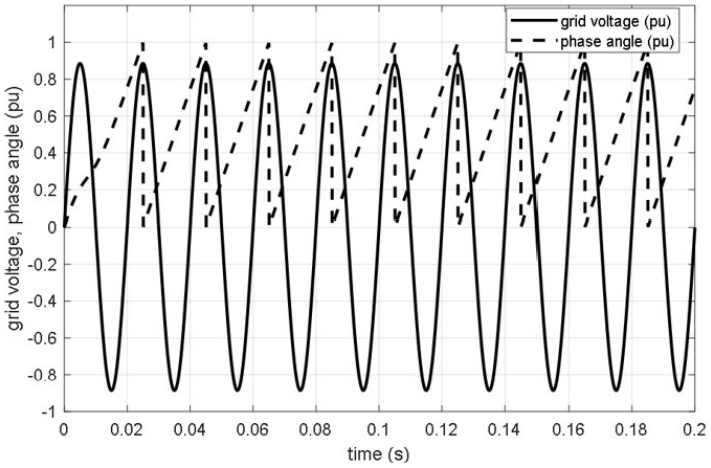


FIGURE 12. Simulation result: Estimated phase angle output of the SOGI-PLL

In this work, the results of the real-time SOGI-PLL algorithm are given from Figure 13 till Figure 17. The real-time model variables observed were the direct and orthogonal output signal from SOGI OSG block, output of Park transform: direct signal (that corelated with the grid voltage magnitude) and quadrature signal, and the main output variables of the SOGI-PLL: the estimated phase and frequency. All the SOGI-PLL variables are observed by using oscilloscope via the external 8-bit DAC connected to the DSC.

Figure 13 shows the direct signal output of the SOGI OSG along with the grid input voltage. It can be seen that the output filter can track the input signal accurately. Whereas the orthogonal signal output of the SOGI OSG is given in Figure 14. (Along with the direct signal). From Figure 14, one can see that the orthogonal signal clearly has 90° phase difference with its direct signal.

The main variable output of the SOGI-PLL that is the estimated phase angle is depicted in Figure 15. To be clearer, the grid voltage signal is also observed. By careful observation from the scope, one can see that the SOGI-PLL could track the grid voltage phase accurately. From the control system of view, this variable is the most important variable that is used by the grid-connected device control systems for the grid synchronization process.

Besides phase angle information, the important variable that is frequently used by the grid-connected device control systems is the grid voltage magnitude information. In the grid-connected renewable energy sources, for example, the grid voltage magnitude generally is used to set the proper DC bus voltage reference. In this work, the result of the estimated voltage magnitude is shown in Figure 16. From the scope, the developed real-time algorithm can detect the voltage magnitude precisely.

The last variable that is observed in this work was the grid voltage frequency. The information of the grid frequency is important mainly in droop or balanced control systems found in the microgrid or distributed generation systems. For the estimated frequency of the grid voltage in this work, the result is shown in Figure 17.

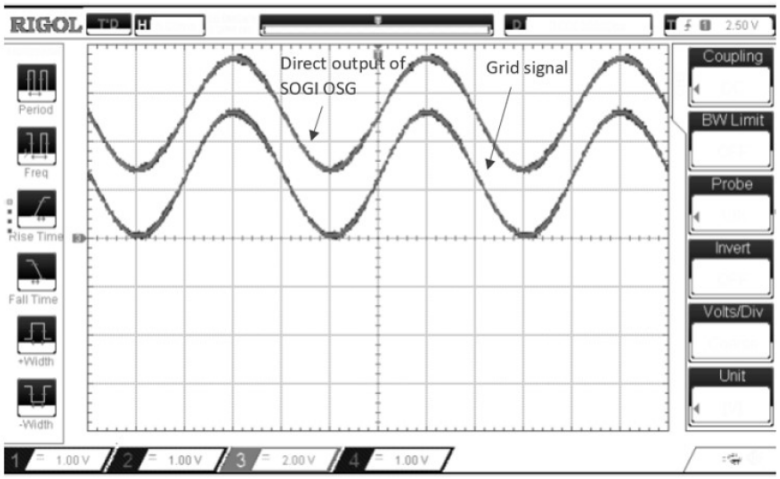


FIGURE 13. Experimental result: Direct output of the real-time SOGI OSG and the grid voltage input

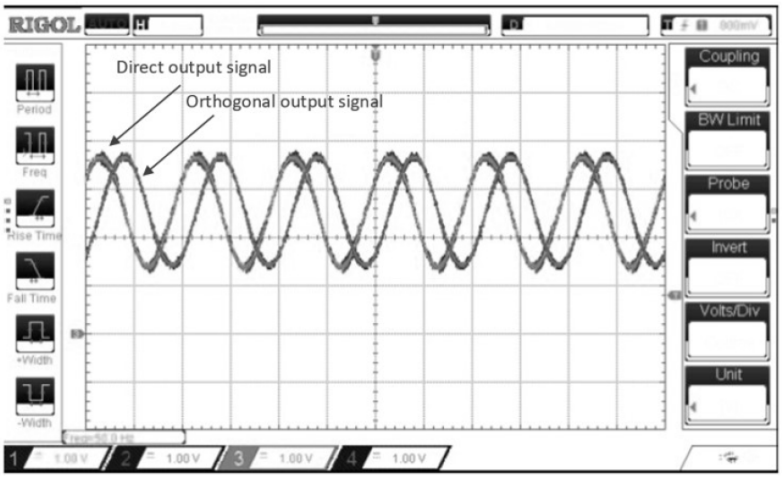


FIGURE 14. Experimental result: Output of the real-time SOGI OSG – Direct output and orthogonal output

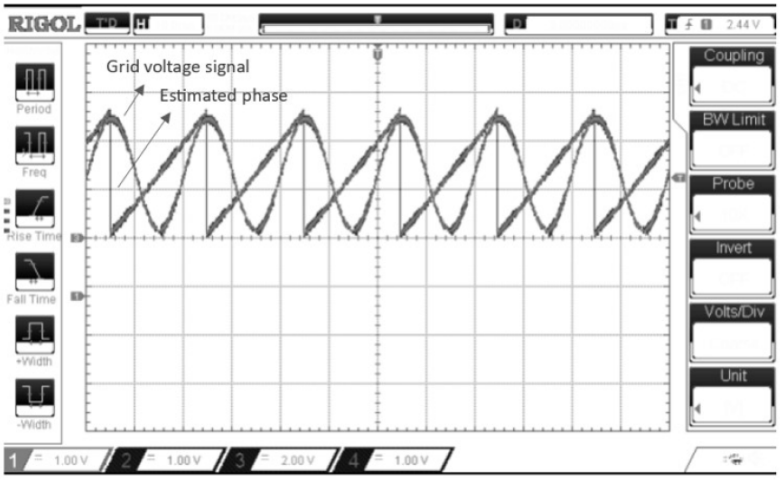


FIGURE 15. Experimental result: Estimated phase angle of the real-time SOGI-PLL

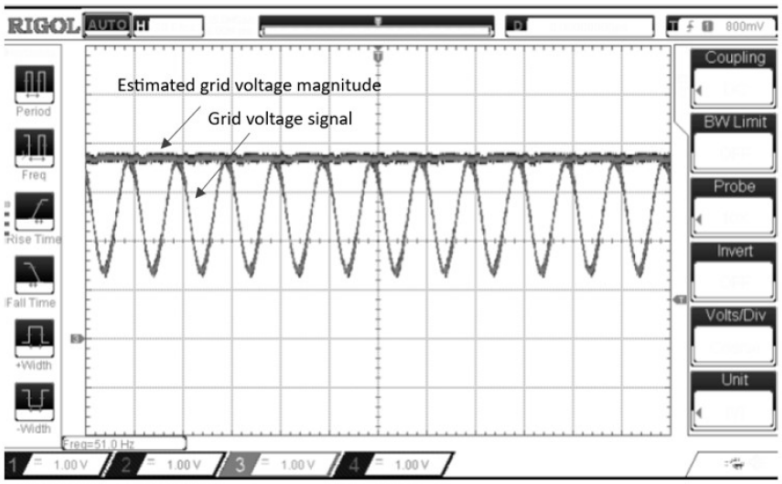


FIGURE 16. Experimental result: Estimated grid voltage magnitude of the real-time SOGI-PLL

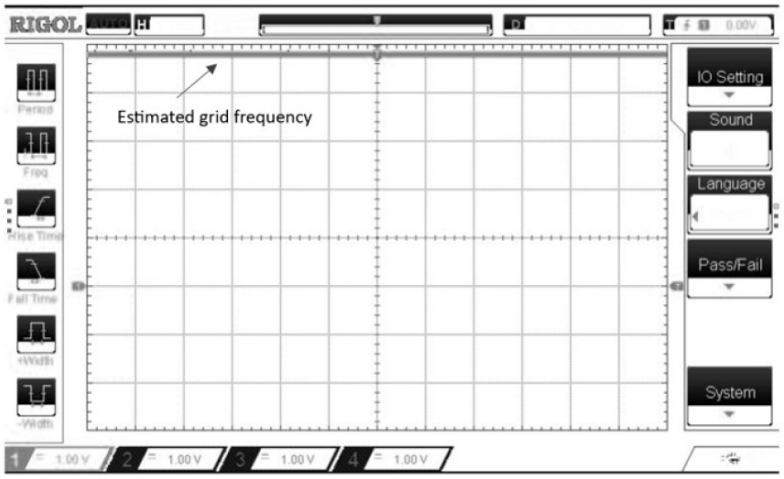


FIGURE 17. Experimental result: Estimated grid voltage frequency of the real-time SOGI-PLL

5. **Conclusions.** This paper presents a practical hard real-time software implementation of SOGI-PLL algorithm. To obtain fast execution time of the algorithm, in this work, the SOGI-PLL is realized using fixed-point arithmetic computation technique and is embedded in 16-bit digital signal processor with 20 MHz crystal oscillator. By using this arithmetic computation technique, the high computation requirement algorithms such as the SOGI-PLL can be implemented using low-cost fixed-point microcontrollers or microcontrollers which have no floating-point processor unit. Based on the testing results, the developed algorithm can estimate the grid voltage parameters accurately.

In this work, it is assumed that the signal of the voltage sensor used in the simulation and experiment is ideal where the grid voltage is purely sinusoidal and has no harmonic distortion, so in this case, more research is needed to investigate the influence of the voltage harmonics to the estimation accuracy. In addition, although the SOGI-PLL method is very adequate for estimating grid voltage parameters in a grid-tied inverter system, if the voltage sensor creates phase delay and/or contains voltage bias, then the estimated variable practically will not only experience a slight oscillation, but the phase estimation also does not represent the actual value. Therefore, it is also necessary to investigate the other advanced PLL topology to overcome that case.

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