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DESIGN AND ANALYSIS OF AN $m+n/k$ MULTIPLIER BASED ON MULTI-PHASE CLOCK

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Abstract. *Multiple clock sources are needed in mobile communication devices to drive each system. As a clock source, the authors have previously proposed a frequency multiplier using a double-edge counter and demonstrated its effectiveness. This paper proposes an* $m+n/k$ *multiplier based on a multi-phase clock. This circuit can realize* $m+n/k$ *multiplication at non-integer frequencies of the input signal by employing the* $1+n/k$ *divider, proposed by the authors, as the basis for the multi-phase clock counting circuit. The characteristics were verified through simulations using Verilog-HDL. It was clarified that the steady-state frequency error of the output signal relative to the input signal frequency corresponds to a one-phase difference of the multi-phase clock. Furthermore, it was confirmed that a regular multiplied signal is obtained within two cycles of the input signal.*

Keywords: Frequency multiplier, Multi-phase clock, Steady-state frequency error, Frequency divider, $m+n/k$

1. **Introduction.**

Systems in mobile communication devices are becoming increasingly complex, and clock signals of various frequencies are needed to drive each system [1, 2, 3, 4]. The main source of these clock signals is a circuit called a phase-locked loop (PLL), which outputs a signal synchronized with the input signal. In recent years, research on PLLs with an all-digital configuration (DPLL: Digital PLL) has been conducted to meet the requirements for circuit integration, stability, and reliability associated with the digitization of various systems [5, 6, 7]. Since an analog PLL is composed of a phase comparator, filter, and voltage-controlled oscillator (VCO), it takes a considerable amount of time for the synchronization state to be achieved when the input signal is applied. When considered as a clock source in mobile communication equipment, etc., it is desirable to stop operation when not in use from the viewpoint of power consumption. Therefore, it

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is desirable to generate a quick clock signal when the system starts up, and analog PLLs have a drawback in this respect. DPLLs that support the generation of quick clock signals have also been researched, but these DPLLs have the disadvantage of not having a wide frequency bandwidth. Thus, multiple designs are required depending on the frequency band used. Multiplication-type DPLLs have also been proposed, but they all have complex circuit configurations and practical problems.

The following characteristics are required for clock signal generation circuits in mobile communication devices:

- Ability to generate clock signals quickly upon system recovery from standby;
- Capability to generate clocks with a 50% duty cycle, as an increasing number of systems utilize both rising and falling edges of the clock signal for signal processing;
- Configuration unaffected by external factors, ensuring system stability;
- Cost-effectiveness through the provision of a general-purpose circuit with a wide frequency bandwidth, thus avoiding the need for separate clock generation circuits for each system.

Multiplier circuits have the above characteristics and can generate various frequencies with a simpler circuit configuration and control scheme than the PLLs described above [8]. However, it is difficult for analog multiplier circuits to generate an output signal with a frequency that is precisely multiplied with respect to the frequency of the input signal. Digital configuration multipliers have also been proposed, but since a single-phase clock is used as the reference clock, a steady-state frequency error of the output signal relative to the input signal occurs for a time width of one cycle of the reference clock at the maximum. In addition, conventional multiplier circuits could only obtain an output signal with an integer multiple of the frequency of the input signal. Therefore, its output frequency was limited for practical use. To improve these problems, a multiplier based on a double-edge counter was proposed [9, 10]. This method uses a double-edge counter that counts both the rising and falling edges of the reference clock as a control counter in the circuit. As a result, the counting error could be less than half the reference clock's period, and the output signal's steady-state frequency error relative to the input signal's frequency can be reduced to half that of the conventional method.

In this paper, we propose an $m + n/k$ multiplier ($k > n$) based on a multi-phase clock. By using a multi-phase clock as the reference clock [11, 12], this circuit can reduce the steady-state frequency error compared to the double-edge counter method. Moreover, by utilizing the $1 + n/k$ divider ($k > n$) previously proposed by the authors as a counting circuit for multi-phase clocks, the circuit achieves an $m + n/k$ multiplier output signal with a non-integer frequency multiplier relative to the input signal. Furthermore, since it is a fully digital configuration, it is easy to integrate and can be expected to be used as a clock supply circuit in various systems.

Chapter 2 describes the circuit configuration and basic operation of the $1+n/k$ divider on which this circuit is based. Chapter 3 describes the circuit configuration of the proposed $m + n/k$ multiplier based on multi-phase clock and its operation analysis. Chapter 4 presents the simulation results using Verilog-HDL. Finally, Chapter 5 presents conclusions.

2. $1 + n/k$ Divider as the Basis of the Proposed Circuit.

2.1. Circuit configuration of $1 + n/k$ divider. The proposed $m + n/k$ frequency multiplier circuit operates by counting the total number of multi-phase clock cycles within one cycle of the input signal and determining the value required for multiplication. The circuit is designed to generate the multiplied output signal by utilizing this value to count the multi-phase clocks. As the multi-phase clock counting circuit, the proposed design employs the $1 + n/k$ divider previously introduced by the authors. Therefore, prior to discussing the proposed circuit, an explanation of the $1 + n/k$ divider is provided.

Figure 1 shows the circuit configuration of the $1+n/k$ divider that forms the basis of the proposed $m + n/k$ multiplier. n is the bit shift value of the ring counter that determines the division ratio, and k is the number of phases of the input signal, a multi-phase clock. This circuit consists of two selectors (selector1, selector2), a ring counter (ring counter) with negative edge operation, a 1/2 frequency divider (1/2), a NOT gate, and an AND gate. In Figure 1, $\mathrm{sel1_{out}}$, $\mathrm{sel2_{out}}$, and $\mathrm{div_{out}}$ are the output signals of selector1, selector2, and 1/2 divider, respectively. The ring counter has only one bit of the output signal high, and each time a clock is applied, its position is shifted n bits to the left, the division ratio. The number of bits in the ring counter is the same as the number of phases k in the multi-phase clock. selector1 connects the output of the ring counter as the selection signal, with one-bit rotated left, and selects the corresponding multi-phase clock. selector2 connects the output of the ring counter as it is as a selection signal, and selects the corresponding inverted multi-phase clock. The multi-phase clock is set so that $T_{mp} = k \cdot t_p$ when the time of one cycle is T_{mp} and the time between each phase is t_p.

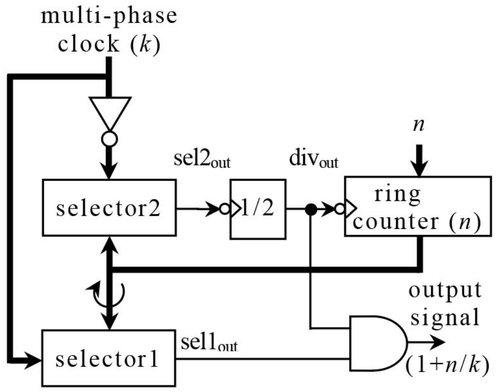

FIGURE 1. Circuit configuration of the $1 + n/k$ divider

2.2. **Operation analysis of $1+n/k$ divider.** Figure 2 shows the operating waveforms of the $1 + n/k$ divider. Now, when the first bit of the ring counter is high at time t_0, selector2 selects multi-phase clock $\mathrm{clk_1}$ and outputs the inverted clock $\mathrm{sel2_{out}}$. In addition,

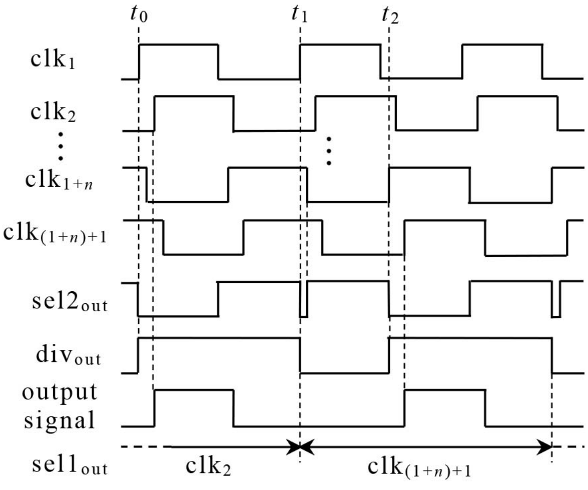

FIGURE 2. Operating waveforms of the $1 + n/k$ divider

selector1 selects multi-phase clock clk_2 by one-bit rotation of the selection signal. At this point, the 1/2 divider goes high on the falling edge of selector2, so clk_2, which is selected by selector1, is output from the AND gate. At the time t_1, the 1/2 divider transitions to a low state at the falling edge of the selector2's output clock $\mathrm{sel2}_{\mathrm{out}}$, causing the ring counter to shift left by n bits. As a result, selector2 selects clk_{1+n}, but its clock is inverted, so $\mathrm{sel2}_{\mathrm{out}}$ remains low. At this time, selector1 selects the next clock $\mathrm{clk}_{(1+n)+1}$ after clk_{1+n}, but since the 1/2 divider is already low, $\mathrm{clk}_{(1+n)+1}$ is never output from the AND gate. Next, at time t_2, the 1/2 divider goes high on the falling edge of the output clock $\mathrm{sel2}_{\mathrm{out}}$ of selector2, so the AND gate outputs $\mathrm{clk}_{(1+n)+1}$, which is selected by selector1. The same operation is repeated below, so the proposed $1+n/k$ divider is a circuit operation that always selects the multi-phase clock n ahead according to the ring counter setting. Next, let us examine the relationship between the input frequency and output frequency of the proposed $1+n/k$ divider. If T_{mp} represents the duration of one cycle of the multi-phase clock, then T_{md}, the duration of one cycle of the output signal, can be expressed as follows:

$$T_{md} = T_{mp} + \left(\frac{T_{mp}}{k}\right) \cdot n = T_{mp}\left(1 + \frac{n}{k}\right) \tag{1}$$

Subsequently, if the frequency of the multi-phase clock is denoted as f_{mp} and the output frequency of the $1+n/k$ divider as f_{out}, then the relationship can be defined as

$$f_{out} = \frac{f_{mp}}{1 + \frac{n}{k}} \tag{2}$$

3. Proposed $m + n/k$ Multiplier.

3.1. Circuit configuration of $m + n/k$ multiplier.

Figure 3 shows the circuit configuration of the proposed $m+n/k$ multiplier. This circuit consists of a $1+n/k$ divider ($k > n$), a $1+z/k$ divider ($k > z$), a 1/2 divider (1/2), five counters (Counter 1∼5), a

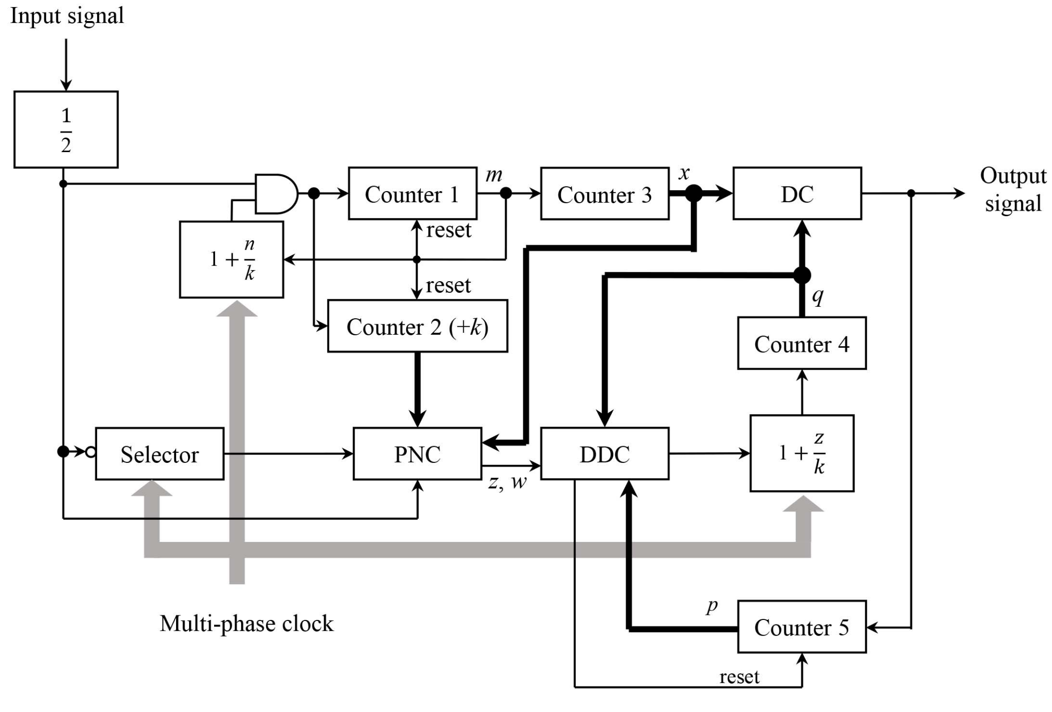

FIGURE 3. Circuit configuration of the $m + n/k$ multiplier

selector (Selector), a digital comparator (DC), a phase number counting circuit (PNC), a $1+z/k$ divider driving control circuit (DDC), and an AND gate. In Figure 3, the thin lines indicate single-bit lines, the thick lines indicate multi-bit lines, and the thick gray lines indicate multi-phase clock inputs. The Selector selects the first multi-phase clock after the output of the 1/2 divider goes low. PNC uses the value of Counter 2 and the multi-phase clock from the Selector to count the number of phases corresponding to the counting error that determines the multiplier operation. DDC switches and controls the operation of the $1+z/k$ divider in three patterns according to the value from PNC and the count of the output signal: dividing by $1+z/k$, dividing by $1+(z+1)/k$, and passing the multi-phase clock as is.

3.2. **Operation analysis of $m+n/k$ multiplier.** Figure 4 shows the operation waveform of the proposed $m+n/k$ multiplier. When the input signal is applied at time t_0, the output of the 1/2 divider goes high, and the AND gate passes the output from the $1+n/k$ divider. The $1+n/k$ divider outputs the multi-phase clock selected at that point as it is until the value of Counter 1 is "$m-1$" and outputs the $1+n/k$ divided signal only when the value is "m". Counter 1 counts up "+1" for each clock. Counter 2 counts up "$+k$" to count the number of phases of multi-phase clocks passing through the AND gate. When Counter 1's value reaches "m", Counter 3 is counted up by "+1", and Counter 1 and Counter 2 are reset. Therefore, the value "x" of Counter 3 counted between time t_0 and t_2 is the value that determines the time width corresponding to "m" in the $m+n/k$ multiplier.

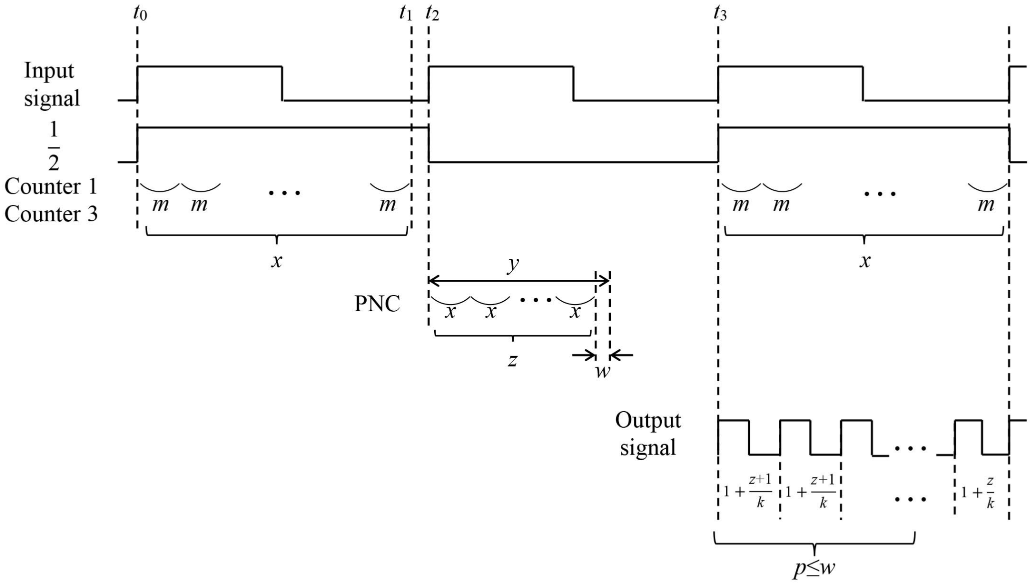

FIGURE 4. Operation waveform of the $m+n/k$ multiplier

Next, consider the counts of each counter between time points t_1 and t_2. During this time, the value of Counter 1 does not reach "m", so the value of Counter 3, "x", remains at time t_1. Therefore, the value of Counter 2 counted between time points t_1 and t_2 is the value that determines the time width corresponding to "n/k" in the $m+n/k$ multiplier. Here, Figure 5 shows the operating waveforms zoomed in between time points t_1 and t_2 in Figure 4. As mentioned above, Counter 2 counts the value corresponding to the number of phases of the multi-phase clock. However, the number of phases is not counted between time points t_1 and t_2 in Figure 5. The number of phases during this period, "j", must also be added to determine the time width corresponding to "n/k". If we define "y" as

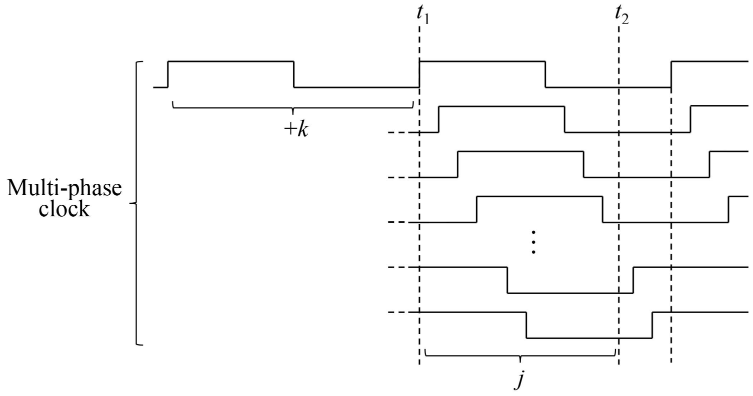

Figure 5. Zoomed in between time points t_1 and t_2 in Figure 4

the number of phases between t_0 and t_2 in Figure 4, PNC repeats counting "$y - x$" until the relationship "$y < x$" is established by the multi-phase clock from the Selector. This repeated value "z" and the remaining phase number "w" corresponding to the remainder are transferred to DDC at the timing of t_3, when the output of the 1/2 frequency divider goes high.

Counter 4 counts the number of clocks from the $1 + z/k$ divider. DDC makes the $1+z/k$ divider perform the desired operation only when the Counter 4 count reaches "x". Otherwise, the multi-phase clock selected at that time is passed through and counted by Counter 4. DC compares Counter 4's counted value "q" with Counter 3's counted value "x", and the output signal is output when "$q = x$".

Here, the value "w" corresponding to the remainder from DDC is the counting error in the operation to determine the multiplier ratio between time t_0 and t_2 in Figure 4. Therefore, if this value is not taken into account in the counting operation to determine the output signal, this leads to a frequency error in the output signal. In the proposed circuit, the number of clocks of the output signal is counted by Counter 5. While this count "p" is "$p \leq w$", DDC sets "$z + 1$" to make the $1 + z/k$ divider perform the desired operation. The above operation distributes the counting error to each period of the output signal and suppresses the frequency error in the $m + n/k$ multiplier.

Based on the above operation, the proposed $m + n/k$ multiplier performs a counting operation to determine the multiplier ratio "m" by Counter 1, Counter 3, and the $1+n/k$ divider in the first cycle of the input signal. In the second cycle, a counting operation to determine "n/k" is performed by Counter 2, Counter 3, the value from the Selector and PNC. In the third cycle, the counted value of PNC is transferred to DDC, and the output signal is generated by Counter 4, Counter 5, $1 + z/k$ divider, and DC. At the same time, the counting operation to determine "m" is restarted. The same operation is repeated in the following steps. From the above, the proposed $m + n/k$ multiplier can generate a multiplied output signal in two cycles after the input signal is applied or the frequency changes.

3.3. **Output frequency and steady-state frequency error.** Next, consider the relationship between the input and output signal frequencies. The time T_{out} of one period of the output signal is the sum of the time of the $x - 1$ period of the multi-phase clock and the time of the clock divided by $1 + z/k$ of the multi-phase clock. Therefore, the time T_{out} of one cycle of the output signal is expressed as

$$T_{out} = (x-1)T_{mp} + \left(1 + \frac{z}{k}\right) T_{mp} \tag{3}$$

Here, "x" corresponds to the value obtained by dividing the time T_{in} of one input signal cycle by the "$m+n/k$" time of the multi-phase clock, which is shown by the following equation.

$$x = \left\lfloor \frac{T_{in}}{\left(1+\frac{n}{k}\right) T_{mp}} \right\rfloor \tag{4}$$

If the number of phases of a multi-phase clock for one input signal period is "y", "z" is equal to the value obtained by subtracting the number of phases corresponding to "x" from the value and dividing it by "x", so that

$$z = \left\lfloor \frac{y - \left(m+\frac{n}{k}\right) x \cdot k}{x} \right\rfloor \tag{5}$$

In addition, "y" can be expressed as

$$y = \left\lfloor \frac{T_{in}}{\frac{T_{mp}}{k}} \right\rfloor \tag{6}$$

Therefore, substituting Equations (4) and (6) into Equation (5), it results in $z = 0$. From this, substituting Equation (3) into Equation (4) and rearranging the equations, the following equation is shown.

$$T_{out} = \frac{T_{in}}{m+\frac{n}{k}} \tag{7}$$

Hence, the following relationship holds if the frequencies of the input and output signals are f_{in} and f_{out}, respectively.

$$f_{out} = \left(m+\frac{n}{k}\right) f_{in} \tag{8}$$

This shows that the proposed circuit can obtain an output signal frequency multiplied by "$m+n/k$" with respect to the input signal.

Next, we consider the steady-state frequency error of the proposed $m+n/k$ multiplier. As described in Section 3.2, the value "z" that determines the time width of the output signal has two states depending on the calculation result: the state in which it remains at "z" and the state in which it is operated at "$z+1$". The time width of the output signal when operated at "z" is expressed by Equation (7). On the other hand, when operating at "$z+1$", the following equation is obtained from Equations (3) to (6).

$$T_{out} = \frac{T_{in}}{m+\frac{n}{k}} + \frac{1}{k} T_{mp} \tag{9}$$

This shows that the steady-state frequency error of the proposed $m+n/k$ multiplier is less than one phase difference of the multi-phase clock.

4. **Simulation Result.**

The operation of the proposed circuit was verified by simulation using Verilog-HDL, a hardware description language.

Figure 6 shows the simulation results from the time an input signal is applied to the proposed multiplier until the multiplier output signal is generated. The number of phases of the multi-phase clock is set to "$k = 7$". The multiplier ratio is set to "$4 + 4/7$" with "$m = 4$" and "$n = 4$", the frequency of the input signal is 20 kHz, and the frequency of the multi-phase clock is 240 kHz.

At time t_0, the input signal is applied. Then, at time t_1, "$x = 7$", which determines the frequency of the multiplied output signal, is determined, and at time t_2, "$z = 6$" is determined. Also, the remainder value "$w = 2$" when calculating "z" is determined at this point. From the explanation of the operation in Chapter 3, it is confirmed that "z",

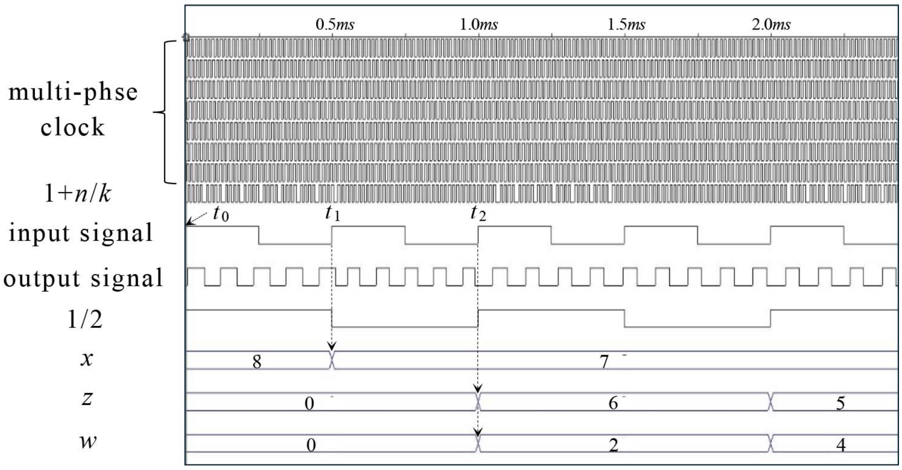

Figure 6. Simulation results from the time an input signal is applied to the multiplier until the output signal is generated

the control value of the $1+z/k$ divider, determines the frequency of the output signal and transition with only two values, "5" and "6" after t_2, the time at which the output signal is generated. This shows that the proposed multiplier exhibits a steady-state frequency error of the output signal corresponding to one phase difference of the multi-phase clock and is capable of generating a multiplied output signal within two periods of the input signal.

Figure 7 shows the simulation results when the input signal frequency changes during the multiplier operation. The multiplier ratio $m+n/k$ is "$4+4/7$" with "$m=4$" and "$n=4$", and the reference clock frequency is 240 kHz. At time t_0, the frequency of the input signal changes from 35 kHz to 20 kHz. Then, at time t_1, "$x=9$", which determines the frequency of the multiplied output signal, is determined, and at time t_2, "$z=5$" and the remainder of the "z" calculation, "$w=3$" is determined t_2. This shows that when the frequency of the input signal changes, the multiplied output signal can be generated within two cycles.

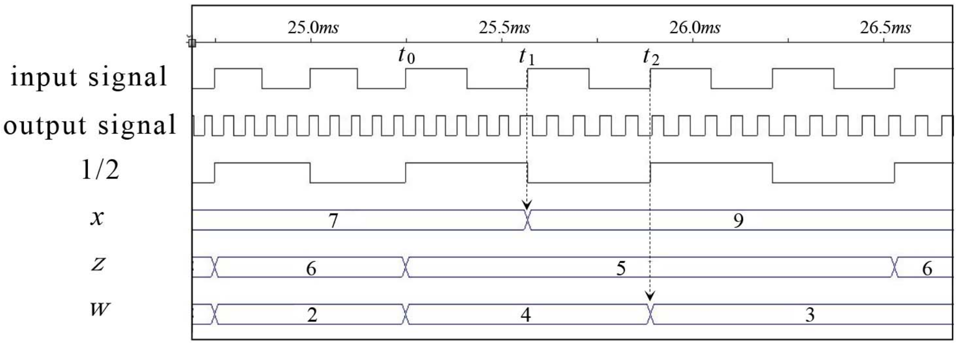

Figure 7. Simulation results when the frequency of the input signal is changed

Simulation has also confirmed that the desired operation can be obtained even when the total number of multi-phase clock, "k", is increased or decreased.

5. **Conclusion.** In this paper, we proposed an $m+n/k$ multiplier using a multi-phase clock. The proposed circuit can obtain "$m+n/k$" multiplier output signals with frequencies other than integer multiples of the input signal by using a $1+n/k$ divider with a

multi-phase clock as the reference clock. The output signal's steady-state frequency error relative to the input signal's frequency can be reduced to less than one-phase difference of the multi-phase clock. In addition, the output signal can be correctly multiplied in two cycles after the input signal is applied. Furthermore, since it is a fully digital configuration, it is easy to integrate and can be used as a clock supply circuit in various systems.

In the future, we aim to implement the proposed circuit as an IC chip and evaluate its performance in terms of usable frequency range and power consumption, comparing it with conventional analog and digital PLLs. Additionally, we aim to explore its application in wearable devices and other technologies in the long term.

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Yujiro Harada obtained his Ph.D. degree in Engineering from Tokai University in 2017. He is currently a full-time assistant professor at the National Institute of Technology, Kurume College, Japan. His main research interests include the A/D converter and the associative memory.

Masaaki Fukuhara received the B.S. degree in Telecommunication Engineering, the M.S. and the Ph.D. degrees in Electrical Engineering from Tokai University, Japan, in 2002, 2004, and 2007, respectively. He has been a lecturer and an associate professor at the School of Information and Telecommunication, Tokai University Takanawa campus since 2013 and 2019, respectively. His main interest is in the application area of neuron MOS technology to improve any electronic and integrated circuit, including CAM (Content Addressable Memory) and FPGA (Field Programmable Gate Array).

Kuniaki Fujimoto graduated from Tokai University (Department of Engineering) in 1987, where he completed master's course in 1989, and was employed as an assistant by Nagasaki Women's Junior College. He was an assistant at Kyushu Tokai University in 1991, and has been a professor at Tokai University since 2010. He received his Ph.D. in Engineering from Tokai University in 2009. His research interests include pulsed circuits and digital circuits.