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# POLYGONAL FIELD PROGRAMMABLE GATE ARRAY USING A NOVEL ROUTING ALGORITHM

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Abstract. *This study proposes a novel routing algorithm for solving switch modules of polygonal Field Programmable Gate Array (FPGA). The dominating set method for Global Routing in symmetrical FPGA has high computational complexity. Consequently, we present a novel low complexity routing algorithm, namely the Mapping Pair (MP) routing algorithm, for solving the problem. An MP is a programmable switch in universal switch modules. All two-pin nets can be searched for their relative MP of switch module through two sub-algorithms of the proposed routing algorithm. The first one is "Searching Neighbor MP Algorithm" and the other is "Searching PMP (Parallel Mapping Pair) Algorithm". The routing is repeated again and again until all 2-pin nets have been fully processed. The experimental results show that the proposed algorithm for polygonal switching architecture can reduce the number of programmable switches in the routing module. As a result, the MP routing algorithm is very useful for any polygonal architecture.*

**Keywords:** Routing algorithm, Field programmable gate array (FPGA), Switch module, Computational complexity

1. **Introduction.** Symmetric FPGA has a high computational complexity when using the dominating set method for Global Routing [5,19,24]. Consequently, this study proposes a simpler switch module routing algorithm, namely the Mapping Pair routing algorithm, for symmetric polygonal FPGA. A typical symmetric FPGA (Field Programmable Gate Array) [2,13,15,20] comprises an array of logic blocks that can be interconnected using routing resources, as shown in Figure 1. Logic circuits are implemented in an FPGA by partitioning logic functions into individual logic modules and interconnecting the logic modules by programming the programmable switches in the routing modules. These logic blocks and routing resources can be configured to implement an arbitrary digital circuit. The routing resources contain many programmable switches. Logic-block (L) includes configurable digital circuits that can implement the logic functions. A typical symmetric FPGA architecture comprises an array of logic modules that can be connected with general routing resources [2,3,21,25-26], as illustrated in Figure 2. The routing resources comprise varying segments of metal wires and two kinds of modules, switch modules and connection modules, which contain user-programmable switches.

A routing module (RM) is the section of the routing resource that would be replicated across the entire symmetric FPGA, and it comprises two connection module (CMs) connected with a switch module (SM). The SM contains many programmable switches for programming them. The CM contains the switch matrix, which is connected to the switch and logic modules. The number of Programmable Switches of a routing module equals the number of programmable switches between two connection modules and a switch module