International Journal of Innovative Computing, Information and Control
Volume 8, Number 8, August 2012
ICIC International ©2012 ISSN 1349-4198
pp. 5899–5916

PERFORMANCE EVALUATION OF LEADING FABLESS INTEGRATED CIRCUIT DESIGN HOUSES BY USING A MULTIPLE OBJECTIVE PROGRAMMING BASED DATA ENVELOPMENT ANALYSIS APPROACH

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Received March 2011; revised August 2011

Abstract. *The fabless integrated circuit (IC) design is one of the most important sectors of the semiconductor industry. In 2010, the total revenue of the fabless IC design sector had already hit US$59.6 billion, accounting for one-fifth of the total semiconductor industry revenue. Thus, understanding the efficiency of fabless IC design houses is critical not only for managers of fabless IC design houses, but semiconductor foundries and investors as well. However, very few researches have tried to benchmark fabless IC design houses. Most existing researches have focused on benchmarking the fabless IC design houses within a particular geographic area, such as Taiwan. Further, very few of the researches that tried to benchmark the world's leading fabless IC design houses introduced the traditional CCR or BCC Data Envelopment Analysis (DEA) models based on improper weight derivations. Such performance evaluation results were derived based on different bases of comparisons of decision-making units (DMUs). Therefore, the purpose of this paper is to evaluate the efficiency of the world's leading fabless IC design houses by introducing a new and reasonable Multiple Objectives Programming (MOP)-based DEA method with derivations of the efficiency achievement measure (EAM). The performance of the world's top forty fabless IC design houses will be evaluated. According to the analytic results, the strength and weakness of IC design houses can be demonstrated and strategies for enhancing the houses can be proposed. In the future, the proposed MOP-based DEA method can serve as an appropriate method for performance evaluations.*
Keywords: Data envelopment analysis (DEA), Fabless IC design house, Multiple objectives programming/efficiency achievement measure (MOP/EAM), Semiconductor industry

1. Introduction.

The notion of performance is a recurrent theme in most branches of management both to academic scholars and practicing managers [1], while the measurement of a firm's productivity efficiency, the multiplication of the technical efficiency and the price efficiency [2] are regarded as some of the most important tasks for managers. Performance evaluation and competitive advantage concern question of how to create the businesses in which a company competes [3,4]. It is important to create superior performance with strategies that are optimized for adaptation (adjusting to differences), aggregation (overcoming differences), arbitrage (exploiting differences), and for compound objectives [5]. Thus, an appropriate measure of productivity efficiency [2] can assist managers in improving a firm's value and enhancing profitability.

However, managers often face problems in measuring firms' performances appropriately. Various efficiency measurement methods have been developed and applied: e.g., Delphi [6], Multiple Criteria Decision Making (MCDM) [7-9], the Analytic Hierarchy Process (AHP) [10], Data Envelopment Analysis (DEA) [11-13]. Among the measurement methods, the DEA methods are the most popular and were widely adopted on national-, industrial-, and firm-level performance evaluations. The traditional DEA models proposed by Charnes et al. [14] or Banker et al. [15] evaluate the performance of DMUs by selecting each DMU's favorable weights. However, such performance evaluation results were derived based on different bases of comparisons of DMUs. Thus, the traditional DEA model is a non-fair model from the aspect of weight derivations.

The fabless integrated circuit (IC) design sector emerged in the 1980s as a result of vertical disintegration in the semiconductor industry. As observed by Macher et al. [16], during the 1980s and 90s, hundreds of fabless IC design houses that design and market semiconductor components, relying on contract manufacturers ("foundries") for the production of their designs (i.e., the fabless/foundry business model), entered into the industry. Fabless IC design houses serve a variety of fast-growing industries, especially the personal computer and communication industries, by offering more innovative designs and shorter delivery times than so-called "merchant semiconductor firms" [16]. According to the Fabless Semiconductors Association (FSA) [13], the revenue of the fabless IC design industry only accounted for US$3.6 billion in 1994 while the revenue of the fabless IC design industry skyrocketed to well over US$ 59.6 billion in 2010 [17]. Apparently, the fabless IC design sector has already accounted for one-fifth of the whole semiconductor industry and played a significant role in the semiconductor value chain. Furthermore, the top thirteen fabless IC design houses are expected to register more than $1.0 billion in sales in 2010. These 13 suppliers are forecast to have a combined $41.4 billion in sales and represent about 70% of the $59.6 billion worth of total revenue of the fabless IC design sector in 2010 [17]. Thus, an understanding of the efficiency of top fabless IC design houses is critical for managers of fabless IC design houses, semiconductor foundries as well as investors.

However, very few researches have tried to benchmark the world's leading fabless IC design houses. Most researches have focused on benchmarking the fabless IC design houses within a particular geographical area, such as Taiwan (e.g., Lu and Hung [18]); however, these contributions are very limited from the perspective of fabless IC design industry analysis since Taiwanese fabless IC design houses accounted for only one-third of the total market. Most leading fabless IC design firms are located in the United States. Further, very limited researches tried to evaluate the world's leading fabless IC design houses (e.g., Chu et al. [19]) by introducing the traditional CCR or BCC DEA models which can be misleading due to improper weight derivations. Such performance evaluation results were derived on unfair bases caused by selections of favorable weights versus inputs and outputs belonging to each DMU. Therefore, the traditional DEA models are not fair due to improper weight derivations. Such non-fair weighting problems in traditional DEA models have further been discussed by Fare et al. [20], Fare and Hunsaker [21], among others. Thus, a performance evaluation of the world's leading fabless IC design houses by the appropriate DEA method(s) can be very helpful for industry managers, investors and academic researchers as well.

To overcome the above-mentioned problems in industry analysis and DEA-based performance evaluations, this research aims to utilize the MOP-based DEA method proposed by Chiang and Tzeng [22] to evaluate the performance of the world's leading fabless IC design firms. Based on the results of a literature review, the authors first summarized the input and output indicators suitable for evaluating the fabless IC design firms (DMUs in this research). Then, the leading fabless IC design firms were evaluated by the CCR, BCC and the MOP-based DEA models using the input and output indicators that were based on summaries of the publicly available financial statements of the firms and industry analysis reports. This introduction of the MOP-based DEA method is expected to assess the efficiency of the firms reasonably since the unfair weights problem mentioned by Fare and Hunsaker [21] can be resolved based on the same weight being associated with the same input or output belonging to all DMUs. The results that were derived by traditional CCR and BCC DEA models will serve as a comparison to demonstrate the discrimination capability of the MOP-based DEA model.

The empirical study will be based on the 2009 financial statements of major listed fabless IC design firms. The empirical study results are expected to demonstrate the efficiency of the newly proposed MOP-based DEA model.

The paper is organized as follows. Literature regarding the performance evaluation, productivity and efficiency of high-technology firms will be reviewed in Section 2. The CCR, BCC and MOP-based DEA methods will be introduced in Section 3. The industrial background and the empirical study process will be presented in Section 4. Section 5 presents a discussion, and Section 6 concludes the research with some final remarks.

2. **Productivity, Efficiency and Performance Evaluation.**

The basic idea of management is to operate a larger number of outputs with fewer inputs in the profit or non-profit organization while performance evaluation is a process of relative performance between inputs and outputs [23]. However, performance evaluation is a difficult task in different organizations [24] while developing and applying useful and consistent tools for performance evaluation and strategy integration direction throughout the organization [25] have become an essential task for modern firms. Thus, firms usually pursue productivity and efficiency through many well-known management tools including benchmarking, reengineering, etc. so as to achieve performance. In the following section, the definitions, past researches about productivity and efficiency as well as their measurement will be described in detail as a basis for developing this research.

Productivity is a measure of outputs from the production process to per unit of inputs and of the ability to create goods and services from a given amount of labor, capital, materials, land, resources, knowledge, time; since capital goods tend to decline in value and wear out in corporations or factories [26]. Quah [27] pointed out that productivity is an aspect of performance, and Wu [28] pointed out that productivity refers to the ratio of output obtained from given inputs such as labor, equipment, capital or land [27]. The other aspects of productivity are efficiency (the relationship of output to the given inputs), effectiveness (the degree of goal attainment), and profitability (the ability to generate an excess money income from output over the monetary costs of inputs for a specific period of time [28]). Generally speaking, the term productivity is defined as the relation of output (i.e., produced goods) to input (i.e., used resources) in the manufacturing transformation process [29].

The terms, productivity and efficiency, have been used frequently in the media over the last ten years by a variety of commentators and often used interchangeably, but this is unfortunate because they are not precisely the same things [30]. Efficiency is commonly defined as the minimum resource level that is theoretically required to run the desired operations in a given system as compared with how much resource that is actually used [31,32].

In science, measurement is the process of obtaining the quantity of a magnitude, such as length or mass, relative to a unit of measurement, such as a meter or a kilogram [33]. The term measurement can also be used to refer to a specific result obtained from the measurement process [34]. Besides establishing conventions for the use of measurement terms, and there are the operational definitions of seven performances words, i.e., effectiveness, efficiency, quality, productivity, quality of work life, innovation, and budget-ability [35]. Among them, measurement of productivity and efficiency has gathered significant interest recently among both academics and practitioners [36].

Productivity measures are with respect to what aspect or aspects of the outputs and inputs are used as a basis of aggregation [37]. The most commonly seen productivity measures include labor productivity index, direct labor cost productivity, capital productivity, direct cost productivity, total cost productivity, foreign exchange productivity, energy productivity, raw materials productivity, etc. Usually, productivity is measured as the ratio of the number of dollars of outputs produced to the number of dollars of inputs [38]. Typical outputs measured include measuring the number of following indicators: (1) research proposals written, (2) papers published, (3) designs produced, (4) products designed, (5) presentations made, (6) patents received, (7) awards won, (8) projects completed, (9) books written [38]. Tangen [29] discussed that there are usually two traditional types of index productivity measures that are distinguished: (1) Partial productivity measures $\pm$ ratios of output to one source of input, such as labour, capital, material or energy. (2) Total productivity measures $\pm$ ratios of total output to the sum of all input factors.

According to Coelli et al. [30], the usual measure of efficiency is used to measure a firm as the ratio of the output(s), and it produces to the input(s), i.e., efficiency = outputs/inputs. However, the formula is often inadequate due to the existence of multiple inputs and outputs related to different resources, activities and environmental factors [39]. The most commonly seen efficiency measurement methods are summarized in Table 1 according to Wu and Ho [40].

Table 1. Efficiency measurement methods

Methods	Approach
Ratio approach	Index between financial statement
Regression analysis	Applying least squares
MCDM	Multiple inputs and outputs
Total factor productivity	Resource allocation efficiency
Balanced scorecard	Combine strategy and key index
DEA	Measuring DMUs

Source: Wu and Ho [40]

Measurement is positioned as the key player for performance evaluation and a central part of each step of the performance improvement planning development. According to Sink and Tuttle [35], when the measurement is done properly, i.e., linked to a purpose or goal that managers and employees have accepted, performance improvement can be driven and motivated. Neely et al. [41] further described performance measurement as the process of a quantification action, where measurement is the process of quantification and action correlates with performance. Performance measures are often used to increase the competitiveness and profitability of manufacturing companies through the support and encouragement of productivity improvements [29].

Performance evaluation means "establishment of measurable objectives and targets through planning requirements and standardized environmental reporting" [25]. Performance evaluation is a complex decision-making problem involving various criteria under the uncertain situations and is defined as the process of quantifying action, or more specifically the process of quantifying and analyzing effectiveness and efficiency [42].

The DEA theory is one of the commonly used performance evaluation method to test, extend, and where necessary, to address productivity and comparative efficiency issues in a host of different organizational environments [39]. The measurement performance by the DEA method that utilized the concept of efficient frontier and DEA's benchmarking is a process of defining valid measures of performance comparison among DMU units [43]. Traditional DEA models being proposed by Charnes et al. [14] or Banker et al. [15] evaluate the performance of DMUs by selecting each DMU's favorable weights. However, such performance evaluation results were derived based on different bases of comparisons of DMUs. Thus, the traditional DEA model is a non-fair model from the aspect of weight derivations. In this research, the MOP based DEA method being developed by Chiang and Tzeng [22] which aims to resolve the above mentioned non-fair weighting problem. Following, the DEA models including the CCR, BCC, and the MOP based DEA methods will be introduced for serving as a basis for the performance evaluation of the world's leading fabless firms in Section 4.

3. **Research Methods.** Data Envelopment Analysis (DEA) has been developed for 30 years. In these periods, many researchers applied the advanced models of DEA. This research not only uses the traditional DEA, but also introduces the MOP with DEA. It is important to select appropriate indicators when measuring the fables IC design house. This research uses the modified Delphi to select the indicators.

3.1. **Modified Delphi method.** The Delphi method was designed by Dalkey and Helmer [44]. After the Delphi method, Murry and Hammous [45] tried to identify issues and problems that were collected from a group of technology education professionals using the Modified-Delphi Technique. The modified Delphi simplified the step of conducting the first round of a survey and replaced the conventionally adopted open style survey [46]. The purpose of the modified Delphi method is to save time, and the experts can focus on research themes, eliminating the need for speculation on the open questionnaire, and to improve the response of the main topic [46,47].

The primary objective of a Delphi inquiry is to obtain a consensus as a minimum of 75 percent agreement on any particular item at of opinion from a group of respondents. Meanwhile, it is possible to develop consensus on a common core of management assessment criteria which, when combined with the institution-, unit-, and position-specific criteria, can form a comprehensive management audit instrument.

The Delphi method originated in a series of studies conducted by the RAND Corporation in the 1950s [48]. The objective was to develop a technique to obtain the most reliable consensus from a group of experts [44]. Delphi may be characterized as a method for structuring a group communication process; so the process is effective in allowing a group of individuals, as a whole, to deal with a complex problem while researchers have developed variations of the method since its introduction [49]. Specific situations have included a round in which the participants meet to discuss the process and resolve any uncertainties or ambiguities in the wording of the questionnaire [48]. The Delphi method proceeds in a series of communication rounds, as follows:

Round 1: Either the relevant individuals are invited to provide opinions on a specific matter, based upon their knowledge and experience, or the team undertaking the Delphi expresses opinions on a specific matter and selects suitable experts to participate in subsequent questionnaire rounds; these opinions are grouped together under a limited number of headings, and statements are drafted for circulation to all participants through a questionnaire [48].

Round 2: Participants rank their agreement with each statement in the questionnaire; the rankings then are summarized and included in a repeat version of the questionnaire [48].

Round 3: Participants re-rank their agreement with each statement in the questionnaire, and have the opportunity to change their score, in view of the group's response; The re-rankings are summarized and assessed for their degree of consensus: if an acceptable degree of consensus is obtained, the process may cease, with the final results then fed back to the participants; if it is not, this third round is repeated [48].

Murry and Hammous [45] modified the traditional Delphi Technique by eliminating the first-round questionnaire containing unstructured questions. It is simplified to replace the conventionally adopted open style survey; doing so is commonly referred to as the modified Delphi method [46]. The modified Delphi technique is similar to the full Delphi in terms of procedure (i.e., a series of rounds with selected experts) and intent (i.e., to predict future events and to arrive at consensus). The major modification consists of beginning the process with a set of carefully selected items. These pre-selected items may be drawn from various sources including related competency profiles, synthesized reviews of the literature, and interviews with selected content experts. The primary advantages of this modification to the Delphi is that it (a) typically improves the initial round response rate, and (b) provides a solid grounding in previously developed work.

Additional advantages related to the use of the modified Delphi technique include reducing the effects of bias due to group interaction, assuring anonymity, and providing controlled feedback to participants [50,51]. Brooks [52] noted that three mailings are usually sufficient in order to arrive at consensus.

3.2. **Data envelopment analysis.** Farrell [2] introduced how to deal with the problem of measuring the productive efficiency to both the economic theorist and the economic policy maker and built the mathematical programming model to discuss the efficiency. DEA is a non-parametric approach and it does not need assumptions about the inputs and outputs. The first DEA model was the CCR model and was proposed by Charnes et al. [14]. It assumes that production exhibits constant returns to scale. Banker et al. extended the model and named the BCC model. It is the case of variable returns to scale [15]. For company managers, controlling the range of inputs and decreasing inputs are easier than increasing the total sales. The CCR and BCC models of DEA are used the input-oriented.

Definition 3.1. *CCR-DEA model computes relative efficiency score (h_i) based on selected s outputs ($r = 1, \ldots, s$) and m inputs ($i = 1, \ldots, m$) using the following linear programming expression [1,19]:*

$$\begin{aligned} &\max h_{ij} = \sum_{r=1}^{s} u_r y_{rj} \Bigg/ \sum_{i=1}^{m} v_i x_{ij} \\ &s.t. \quad \sum_{r=1}^{s} u_r y_{rj} \Bigg/ \sum_{i=1}^{m} v_i x_{ij} \leq 1 \\ &u_r, v_i \geq \varepsilon > 0; \quad r = 1, \ldots, s; \quad i = 1, \ldots, m; \quad j = 1, \ldots, n. \end{aligned} \tag{1}$$

In (1), it assumes the DMU has s outputs and m inputs, and there are n DMUs. The u_r and v_i are not zero, calculating as $u_r, v_i \geq \varepsilon > 0$, ε is non-Archimedean number and is 10^{-6}.

Definition 3.2. *Input-oriented BCC has a variable u_0 (returns to scale). The mathematical programming shows as follows [15]:*

$$\begin{aligned}
&Assuming \ \left(\sum_{i=1}^{m} v_i x_{ij}\right) = 1 \\
&\max h_{ij} = \left(\sum_{r=1}^{s} u_r y_{rj} - u_0\right) \Big/ \left(\sum_{i=1}^{m} v_i x_{ij}\right) \\
&s.t. \quad \left(\sum_{r=1}^{s} u_r y_{rj} - u_0\right) \Big/ \left(\sum_{i=1}^{m} v_i x_{ij}\right) \leq 1, \\
&u_r, v_i \geq \varepsilon > 0; \quad r = 1, \ldots, s; \quad i = 1, \ldots, m; \quad j = 1, \ldots, n.
\end{aligned} \tag{2}$$

Equation (2) was changed to (3) for solving formula by using the fractional mathematical programming approach as follows:

$$\begin{aligned}
&\max g_j = \left(\sum_{r=1}^{s} u_r y_{rj} - u_0\right) \\
&s.t. \quad \sum_{i=1}^{m} v_i x_{ij} = 1 \\
&\sum_{r=1}^{s} u_r y_{rj} - \sum_{i=1}^{m} v_i x_{ij} - u_0 \leq 0 \\
&u_r, v_i \geq \varepsilon > 0; \quad r = 1, \ldots, s; \quad i = 1, \ldots, m; \quad j = 1, \ldots, n.
\end{aligned} \tag{3}$$

The dual formula:

$$\begin{aligned}
&\min Z_j = \theta - \varepsilon \left(\sum_{i=1}^{m} s_i^- + \sum_{r=1}^{s} s_r^+\right) \\
&s.t. \quad \sum_{j=1}^{n} \lambda_j x_{ij} - \theta x_{ij} + s_i^- = 0, \\
&\sum_{j=1}^{n} \lambda_j y_{rj} - s_i^- = y_{rj}, \\
&\sum_{j=1}^{n} \lambda_j = 1 \\
&\lambda_j, s_i^-, s_r^+ \geq 0; \quad r = 1, \ldots, s; \quad i = 1, \ldots, m; \quad j = 1, \ldots, n.
\end{aligned} \tag{4}$$

3.3. **Multiple objectives programming (MOP) based DEA method.** The MOP based DEA provides a unitary weight (u^*, v^*) for all DMU, which are evaluated by an equal standard [22]. By this approach, we can obtain the efficiency rating of each DMU more fairly. Moreover, all DMU can be treated simultaneously, which makes it effective in handling large numbers of DMU.

Model 1:

$$\begin{aligned}
&\max z_1 = \sum_{r=1}^{s} u_r y_{r1} \Bigg/ \sum_{i=1}^{m} v_i x_{i1} \\
&\max z_2 = \sum_{r=1}^{s} u_r y_{r2} \Bigg/ \sum_{i=1}^{m} v_i x_{i2} \\
&\qquad \vdots \\
&\max z_n = \sum_{r=1}^{s} u_r y_{rn} \Bigg/ \sum_{i=1}^{m} v_i x_{in} \\
&s.t. \quad \sum_{r=1}^{s} u_r y_{rj} \Bigg/ \sum_{i=1}^{m} v_i x_{ij} \leq 1 \\
&\quad u_r, v_i \geq \varepsilon > 0; \quad r = 1, \ldots, s; \quad i = 1, \ldots, m; \quad j = 1, \ldots, n.
\end{aligned} \tag{5}$$

The definition of y_{rj} is the observed amount of output of rth ($r = 1, 2, \ldots, s$) type for the jth DMU ($j = 1, \ldots, n$). The x^{ij} is the observed amount of input of rth ($r = 1, 2, \ldots, s$) type for the jth DMU ($j = 1, \ldots, n$). The v_i is the multiplier or weight of the ith input and the u_r is the multiplier or weight of the rth output. The ε is non-Archimedean quantity.

Then multiply the numerators and denominators in CCR model [14] was established the multiple objectives programming model and shown as Equation (5). It was considered by the efficiencies of all DMU and established a Multiple Objective Linear Fractional Programming (MOLFP) model, as shown in Model 1 (Equation (5)). According to the research of Sakawa and Yumine [9], Sakawa and Yano [8], and Ohta and Yamaguchi [53], the MOLFP problem can be solved by the Multiple Objective Linear Programming (MOLP) approach, as proposed by Zimmermann [54]. MOLP with DEA approach adopts to obtain common weights, which can maximize all DMU's efficiencies.

The concept of MOLP utilizes membership function transfers of multiple objective functions into one objective function. The membership function is as follows:

$$\mu_j(z_j) = \begin{cases} 0; & z_j \leq z_j^L \\ \dfrac{z_j - z_j^L}{z_j^R - z_j^L}; & z_j^L \leq z_j \leq z_j^R \\ 1; & z_j \geq z_j^R \end{cases}$$

where z_j^L and z_j^R are the negative ideal solution and the positive ideal solution, respectively, for the value of the objective function z_j, such that the degree of membership function is $[0, 1]$. The geometric view of the linear membership function is shown in Figure 1.

The degree of membership function of z_j in $\mu(z_j)$ refers to the achievement level of the efficiency ratio for DMU_j .The problem of obtaining the maximum decision is to choose (μ^*, v^*), such that

Model 2:

$$\begin{aligned}
&\max_{u,\omega} \min_{j} u(z_j) \geq \alpha; \quad j = 1, \ldots, n. \\
&s.t. \quad \left(\sum_{r=1}^{s} u_r y_{rj}\right) \Bigg/ \left(\sum_{i=1}^{m} v_i x_{ij}\right) \leq 1; \quad j = 1, \ldots, n \\
&u(z_j) \geq \alpha; \quad j = 1, \ldots, n.
\end{aligned} \tag{6}$$

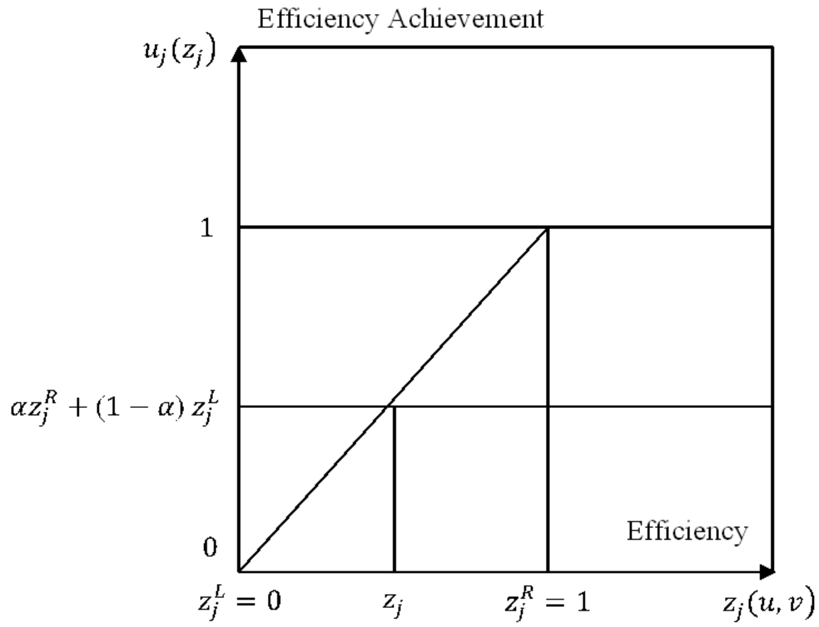

FIGURE 1. Linear membership function of z_k

Then, let the achievement level of the objective functions for Model 1 to be at a larger level, such as:

$$\alpha = \left(z_j - z_j^L\right) / \left(z_j^R - z_j^L\right) . \tag{7}$$

Equation (7), via variable transformation, has transformed $z_j = \alpha \cdot z_j^R + (1-\alpha) \cdot z_j^L$ where z_j is a convex combination of z_j^L and z_j^R; (7) can be rewritten as (8). According to the concept of multiple objective linear programming, we can determine a weight that satisfies all DMU restrictions. The weight (μ^*, v^*), is the common weight of all DMU, which are evaluated on a consistent standard of ranking.

$$\begin{aligned} &\underset{\mu,v}{\text{Max}}\ \underset{j}{\text{Min}} \left\{ Z_j = \left(\sum_{r=1}^{s} \mu_r y_{rj}\right) \Big/ \left(\sum_{i=1}^{m} v_i x_{ij}\right) \right\} \\ &\quad s.t. \quad \left(\sum_{r=1}^{s} \mu_r y_{rk}\right) \Big/ \left(\sum_{i=1}^{m} v_i x_{ik}\right) \le 1 , \\ &\quad \left(\sum_{r=1}^{s} \mu_r y_{rj}\right) \Big/ \left(\sum_{i=1}^{m} v_i x_{ij}\right) \ge \alpha \cdot z_j^R + (1-\alpha) \cdot z_j^L \\ &0 \le \alpha \le 1 \\ &u_r \ge \varepsilon > 0, \quad r = 1, 2, \ldots, s \\ &v_i \ge \varepsilon > 0, \quad i = 1, 2, \ldots, m \end{aligned} \tag{8}$$

The efficiency approach measure (EAM) is

$$\alpha_k = \left(\sum_{r=1}^{s} u_r^* \times y_{rk}\right) \Big/ \left(\sum_{i=1}^{m} v_i^* \times x_{ik}\right) \tag{9}$$

4. **Evaluating the World's Leading Fabless IC Design Houses by the MOP Based DEA.** In this section, the industry background of the fabless IC design houses will be introduced to serve as the background for the research. Next, the top 40 fabless IC design houses will be selected as DMUs. Then, the modified Delphi method being

proposed by Murry and Hammous [45] will be used to select the input and the output indicators for the CCR, BCC and MOP-based DEA models. After that, the selected indicators will be applied to calculate the efficiency scores. Detailed procedures and the performance evaluation results are illustrated below.

4.1. **Background of the fabless IC design industry.** The fabless IC design industry is a part of the semiconductor industry, and the fabless model will continue to thrive as long as fabless companies leverage the model to focus on the key qualities for success [55]. According to the statistical data published by the Global Semiconductors Alliance (GSA), the revenue of the fabless industry was merely $2.4 billion dollars in 1993; whereas in 2009, the total revenue exceeded $56.6 billion [56,57].

IC design houses can be classified into three categories: fabless IC design houses, system houses, and integrated device manufacturers (IDMs). Fabless IC design houses (without a semiconductor fabrication, or fab) are usually business models that outsource the manufacturing of silicon wafers and focus on the IC design, development and marketing of their products and form alliances with silicon wafer manufacturers or foundries [58]. The IDM is a class of semiconductor companies that owns an internal silicon wafer fab, or as the name indicates, the fabrication of wafers is integrated into its business [58].

In 2009, 74% of the global fabless revenue was generated by the top 40 houses, which are distributed primarily in the U.S., Taiwan and United Kingdom. The top five IC design houses account for about 60% of the top 40 IC design houses.

4.2. **Performance evaluation of the fabless IC design industry.** In the following, the performance evaluation procedure of the top 40 fabless IC design firms (Table 2) will be introduced. At first, the firms were selected according to the "Annual Semiconductor Report" by FSA. The firms will serve as the DMUs in the evaluation. Then, possible financial indicators for serving as the inputs and outputs of the MOP-based DEA model were selected based on literature review results. The financial indicators were further confirmed by an accounting professor for suitability. Following that, the modified Delphi method that was introduced in Section 3.1 was utilized to derive the input and output indicators for the DEA model based on the opinions of 15 experts from the Taiwanese IC industry. At that point, two input indicators and three output indicators were derived. The input indicators that were derived include "cost of goods sold" and "R&D expenses", while the output indicators include "total revenue", "ROI" and "profitability".

The 2009 financial data for the input and output indicators (see Table 3) were downloaded from the websites of the NASDAQ, the NYSE, and the Taiwan Market Observation Post System. Then, according to the MOP-based DEA model that was introduced in Section 3.3, the weights associated with the input and output indicators were derived by using the Lingo 8.0 [59] as demonstrated in Table 4.

Finally, the efficiency scores and the ranking order for each DMU that was derived by using the CCR, BCC and MOP-based DEA models, respectively, are demonstrated in Table 5. In the CCR and BCC models, the efficiency scores of more than 10 firms are equal to 1. Broadcom, Nvidia, Marvell and LSI logic are ranked as the top 2, 4, 5 and 6, respectively, from the aspect of total revenues. However, the efficiency scores obtained from the traditional CCR, BCC, and the MOP-based DEA models are much lower than those of firms with lower revenue and are ranked from 10 to 13.

5. **Discussion.** In this research, a novel MOP-based DEA model was introduced for benchmarking fabless IC design houses. Very different performance evaluation results have been derived in comparison to those derived by traditional CCR and BCC models as well as those of the earlier researches that were based on the traditional CCR and BCC models

TABLE 2. Top 40 fabless firms' rank/nationality/revenue in 2009

(unit: US$ million)

Rank	Firms	Nationality	2009 Revenue	2008 Revenue	Growth Rate (%)
1	Qualcomm	US	10416	11142	-6.50%
2	Broadcom	US	4490	4658	-3.60%
3	MediaTek	Taiwan	3756	2995	25.40%
4	Nvidia	US	3326	3425	-2.90%
5	Marvell	US	2808	2951	-4.90%
6	LSI Logic	US	2219	2677	-17.10%
7	Xilinx	US	1834	1825	0.40%
8	Avago	US	1484	1699	-12.70%
9	Altera	US	1195	1367	-12.60%
10	Novatek	Taiwan	829	834	-0.70%
11	Himax	US	692	833	-16.90%
12	Realtek	Taiwan	662	566	16.80%
13	CSR	UK	601	695	-13.50%
14	MegaChips	Japan	564	490	14.90%
15	Sunplus	Taiwan	550	527	4.30%
16	Qlogic	US	549	634	-13.40%
17	Atheros	Taiwan	542	472	14.80%
18	PMC-Sierra	Canada	496	525	-5.50%
19	Silicon Labs	US	441	416	6.00%
20	Zoran	US	380	439	-13.40%
21	SMSC	US	308	326	-5.80%
22	Semtech	US	287	295	-3.10%
23	SSTI	US	252	316	-20.30%
24	Etron	Taiwan	230	253	-9.50%
25	Zarlink	US	227	183	24.00%
26	Cirrus Logic	US	221	175	25.70%
27	Power Integrations	US	216	202	6.40%
28	DSP Group	US	212	306	-30.70%
29	Conexant	US	208	332	-37.30%
30	Sigma Designs	US	206	209	1.40%
31	AMCC	US	206	214	-4.20%
32	Lattice	US	194	222	-12.60%
33	Actel	US	191	218	-12.80%
34	VIA	Taiwan	179	274	-35.00%
35	Vitesse	US	168	229	-26.60%
36	ISSI	US	154	235	-34.50%
37	Sitronix	Taiwan	152	205	-25.90%
38	Silicon Image	US	151	274	-45.20%
39	SiRF	US	138	Private	Private
40	Wolfson	UK	121	198	-38.90%

Source: From Global Semiconductor Alliance [56] and company data
Remark: SiRF was acquired by CSR in 2009 and did not have public financial report.

TABLE 3. The values of the input and output indicators

Indicator / Firm	Cost of Goods Sold	R&D Expense	Total Revenue	ROI	Profitability
Qualcomm	3181.00	2440.00	10416.00	0.23	-0.50
Broadcom	2210.60	1534.92	4490.32	0.03	-0.70
MediaTek	1443.14	731.79	3756.31	0.43	0.69
Nvidia	2149.52	908.85	3326.45	-0.06	-1.27
Marvell	1227.10	813.13	2807.69	0.18	1.40
LSI Logic	1375.80	608.31	2219.16	-0.18	0.92
Xilinx	669.20	355.39	1825.18	0.32	0.00
Avago	924.00	245.00	1484.00	0.17	-1.77
Altera	396.60	256.10	1195.41	0.19	-0.30
Novatek	568.85	97.06	828.96	0.29	0.07
Himax	550.60	71.36	692.38	0.14	-0.48
Realtek	361.30	120.47	661.66	0.21	1.32
CSR	333.10	169.70	601.40	-0.03	-1.18
MegaChips	466.73	17.16	563.98	0.32	0.13
Sunplus	370.96	120.78	550.13	0.08	5.40
Qlogic	196.13	137.83	549.07	0.24	-0.49
Atheros	278.87	130.59	542.47	0.05	1.44
PMC-Sierra	165.20	149.18	496.14	0.25	-0.63
Silicon Labs	161.27	104.39	441.02	0.15	1.21
Zoran	196.50	112.19	380.08	-0.09	0.85

Indicator / Firm	Cost of Goods Sold	R&D Expense	Total Revenue	ROI	Profitability
SMSC	154.85	77.70	307.78	-0.08	-0.84
Semtech	131.51	44.85	286.56	0.22	-0.97
SSTI	177.09	43.16	252.33	-0.05	0.74
Etron	189.09	19.47	229.68	-0.01	1.04
Zarlink	118.20	46.00	227.20	-0.47	0.01
Power Integrations	107.63	30.47	215.70	0.16	10.64
DSP Group	133.59	56.15	212.19	-0.34	0.96
Conexant	86.70	51.35	208.43	-0.23	-118.00
Sigma Designs	114.38	52.64	206.08	0.02	-0.91
AMCC	92.93	88.10	205.60	-0.11	0.95
Lattice	90.08	56.13	194.42	-0.04	0.82
Actel	90.86	60.72	190.63	-0.15	-2.85
VIA	102.46	88.32	178.79	-1.41	0.30
Cirrtus Logic	77.46	44.31	174.64	0.03	0.16
Vitesse	78.41	45.69	168.18	-4.54	-25.26
ISSI	113.37	20.02	154.25	-0.06	0.72
Sitronix	112.54	17.85	152.27	0.21	-0.07
Silicon Image	69.79	68.23	150.59	-0.72	-13.91
Elan	91.61	27.57	145.14	0.98	1.70
Wolfson	59.85	44.01	121.33	-0.14	-2.39

Remark: The unit for cost of goods sold, R&D expenses and total revenue is $million

Table 4. Weights versus the indicators

EAM	**Cost of Goods Sold**	**R&D Expense**	**Total Revenue**	**ROI**	**Profitability**
Weights	11.28	13.36	23.62	0.10	6.40

(e.g., Chu et al. [19]). According to the performance evaluation results, the top ranking firms with the highest revenues (e.g., Broadcom, Nvidia, Marvell, LSI Logic) do not always achieve optimal efficiencies in all three DEA models. This phenomenon merits discussion. Further, some of the leading fabless design houses share some common characteristics (e.g., nationality, target markets of products) and demonstrate the same tendencies in performance. Detailed discussion will be very helpful to the firms' management in the future. In the following Section, discrepancies in the comparison results, managerial implications and advances in research methods will be discussed.

First, the differences between the comparison results will be discussed. The results of the efficiency scores and ranking orders for each DMU that is derived by using the CCR, BCC, and the MOP-based DEA models are demonstrated in Table 5. Based on the evaluation results that were derived by the CCR and the BCC models, more than 10 design houses achieved optimal performance. Only three firms – Altera, Semtech and Power Integration – achieved the optimal efficiency score by using the same weights that were derived from the MOP-based DEA model. Fabless design houses such as Xilinx and MegaChips can be recognized as performance maximizers based on the results derived by using the CCR and BCC DEA models; however, the performance evaluation results of the firms could be far below optimal. The major reason for such significant discrepancies is due to the traditional DEA models' efficiency measurements of the favorite weights being associated with each DMU, whereas the MOP-based DEA models derive the same weights for every DMU. Apparently, the discriminant capability of the proposed MOP-based DEA model is much better.

Some leading fabless IC design houses like Broadcom, Nvidia, Marvell, LSI Logic, and CSR are ranked 2, 4, 5, 6, and 13 from the aspect of revenues; however, their efficiency scores are lower than those of other firms based on the evaluation results by either traditional DEA models or the MOP-based DEA model. Some reasons for this are straightforward. According to Table 2, the cost of goods sold versus the total revenue ratio and/or the R&D expense versus the total revenue ratio of some less competitive firms (e.g., Nvidia and LSI Logic) are much higher than those of other high-performing firms. Other possible reasons include 1) the optimal mix of inputs has not been achieved due to the failure in production planning, marketing and sales capability; 2) an inappropriate pricing mechanism causing lower revenues; or 3) comparatively lower than average workforce productivity. To resolve the above-mentioned reasons for the below-average performances, there should be a review and reconfiguration of the marketing mix strategies, supply chain strategies, and R&D human resources management strategies.

To further explore the nature of the firms from the aspect of target markets, the firms targeting at the PC market (e.g., Nvidia, Via, Realtek, SMSC), consumer electronics (e.g., Sunplus), LCD driver and controller (e.g., Novatek, Himax) and tier two multimedia and communication chip vendors (e.g., Sunplus, Realtek, Atheros), are less profitable. Apparently, it would be very helpful for the firms to target a more appropriate market segment by redefining their R&D portfolio. Meanwhile, the top management of the firms should focus on how innovation strategies can be introduced for rolling out radical/disruptive innovative products instead of just providing incremental innovative products or "me too" substitutes for the products of the firms with best performance scores.

Table 5. Traditional CCR, BCC efficiency and the MOP based DEA method (two input indicators and three output indicators)

NO.	DMU	CCR	Rank	BCC	Rank	MOP	Rank
1	Qualcomm	1.00	1	1.00	1	0.98	4
2	Broadcom	0.65	39	0.65	40	0.64	37
3	MediaTek	0.98	14	1.00	1	0.93	8
4	Nvidia	0.64	40	0.70	37	0.59	39
5	Marvell	0.75	32	0.75	33	0.74	24
6	LSI Logic	0.65	38	0.67	39	0.61	38
7	Xilinx	1.00	1	1.00	1	0.97	5
8	Avago	0.83	27	0.91	22	0.71	29
9	Altera	1.00	1	1.00	1	1.00	1
10	Novatek	0.89	23	0.90	23	0.72	25
11	Himax	0.83	26	0.84	27	0.65	35
12	Realtek	0.85	25	0.86	26	0.79	21
13	CSR	0.68	37	0.68	38	0.68	34
14	MegaChips	1.00	1	1.00	1	0.70	31
15	Sunplus	0.70	36	0.70	36	0.65	35
16	Qlogic	0.97	15	0.98	15	0.93	8
17	Atheros	0.77	30	0.77	31	0.76	23
18	PMC-Sierra	1.00	1	1.00	1	0.89	11
19	Silicon Labs	0.99	13	1.00	14	0.96	6
20	Zoran	0.74	34	0.74	34	0.72	25
21	SMSC	0.81	29	0.81	29	0.80	18
22	Semtech	1.00	1	1.00	1	1.00	1
23	SSTI	0.76	31	0.76	32	0.72	25
24	Etron	0.94	18	0.97	17	0.72	25
25	Zarlink	0.88	24	0.89	25	0.87	12
26	Power Integrations	1.00	1	1.00	1	1.00	1
27	DSP Group	0.73	35	0.73	35	0.71	29
28	Conexant	1.00	1	1.00	1	0.95	7
29	Sigma Designs	0.82	28	0.82	28	0.78	22
30	AMCC	0.90	21	0.94	20	0.70	31
31	Lattice	0.92	20	0.93	21	0.85	14
32	Actel	0.89	22	0.89	24	0.80	18
33	VIA	0.74	33	0.77	30	0.58	40
34	Cirrus Logic	1.00	1	1.00	1	0.93	8
35	Vitesse	0.93	19	0.96	19	0.81	16
36	ISSI	0.97	16	0.97	18	0.80	18
37	Sitronix	1.00	1	1.00	1	0.82	15
38	Silicon Image	0.96	17	0.98	16	0.70	31
39	Elan	1.00	1	1.00	1	0.86	13
40	SiRF	N/A(*)	N/A(*)	N/A(*)	N/A(*)	N/A(*)	N/A(*)
41	Wolfson	1.00	1	1.00	1	0.81	16

Note.(*): N/A: SiRF was acquired by CSR in 2009 and did not have public financial report.

From the aspect of the nationality of the fabless IC design houses, most fabless IC design houses are located in the U.S., Taiwan, and the U.K.; however, for Taiwanese fabless design houses (e.g., Mediatek, Novatek, Himax, Realtek, Sunplus), the majority of the firms are less competitive than the U.S. and U.K. firms, based on the performance scores derived by the MOP-based DEA. One possible reason may be due to the Taiwanese firms' development of low-cost substitutes to the innovative products being provided by the leading U.S. firms. Except for a very few Taiwanese firms like Mediatek (the Taiwanese fabless IC design house providing 2.5G/2.75G handset chipsets as well as optical storage chips and digital TV chips), which is a subsidiary of the world's leading semiconductor foundry, United Microelectronics Corp., and which can control their cost efficiently while developing state-of-the-art products by recruiting the best engineers with competitive bonus programs, other Taiwanese firms usually suffer from the lower prices and higher cost structure due to their limited scale. Thus, government officers should consider how the national innovation system can be reconfigured and the innovation policy redefined so as to enhance the profitability of the firms.

For the advantages of the MOP-based DEA framework, liner programming was introduced to derive the same weights versus input and output indicators. Thus, the performance evaluation results are more fair and reasonable. Further, based on the performance evaluation results, only three firms achieved optimal efficiency in comparison to the results derived by the CCR and BCC models. Apparently, the MOP-based DEA method has demonstrated higher discriminant capabilities than the CCR and BCC models [22] which measure the DMUs with their favorite weights.

Finally, the contributions, limitations and future research possibilities will be discussed. The contributions of this research are twofold. On the one hand, this research contributes to the industry analysis of fabless IC design. On the other hand, earlier researches have either focused on firms within a particular geographical area (e.g., the earlier work by Lu and Hong in 2009 [18]) or by using traditional CCR and BCC methods (e.g., the earlier work by Chu et al. in 2008 [19]). The contributions of these studies that focus on a particular geographical area are very limited since they do not provide a complete picture. The value of such research is very limited from the viewpoint of investment or industry analysis. Moreover, the results derived by using the traditional CCR and BCC models are not fair since the results are not derived based on similar weights versus the evaluation criteria. Apparently, this research can provide future researchers with an overview of the leading fabless design houses with appropriate performance evaluation results.

As for the major limitations of this research, the differences between the accounting systems used in different nations decreases the generalizability of this research. The input and output indicators came from different accounting systems and public markets (NASDAQ, NYSE, and Taiwan Market Observation Post System are major public markets among the top 40 fabless firms); for example, the firms listed on the Taiwan stock market (e.g., Mediatek, Novatek, Via, Sunplus) use the accounting standards developed by the Accounting Research and Development Foundation in Taiwan. Different accounting standards may affect the input and output indicators.

The financial data of this study were obtained from annual financial reports of the companies in 2009. Nearly all industries were affected by the global financial crisis in 2008. IC fabless design houses also faced a severe downturn as a consequence of this crisis. Firms' top management may respond to the depression by adjusting their input mix or R&D expenditures. Different strategies for adjustment in the recession may affect firm performance. Thus, in future studies, the Malmquist productivity index (MPI) can be introduced to measure the efficiency of firms in different economic cycles (i.e., booms vs. recessions). Meanwhile, the proposed MOP-based DEA model can be applied on all other performance evaluation problems and provide highly trustworthy results.

6. Conclusions and Future Research.

Firm performance is a critical issue of concern, both for the firms themselves and for their stakeholders. According to the performance evaluation results, firms can compare themselves with others in the same industry and then develop strategic plans for enhancing their performance. Over the past decades, many performance evaluation models have been developed. Various DEA models have been applied extensively by researchers. Nevertheless, one of the major problems of these studies that use the traditional DEA models is their selection of favorable weights versus each DMU. Thus, performance evaluation results may be biased due to unrealistic weight distributions. To resolve these unfair weighting problems, the MOP-based DEA model was proposed. In contrast to the traditional DEA models, the MOP-based DEA method is capable of deriving the same weight for each DMU, thereby achieving better discriminant capabilities.

Based on the empirical study results, Altera, Semtech and Power Integration were found to be the most efficient firms. Furthermore, U.S. fabless design houses are more competitive than Taiwanese firms, which tend to provide "me too" products that target inappropriate market segments and use over-expensive wafers. To remedy this situation, appropriate innovation policy as well as innovation, R&D and supply chain strategies should be adopted by government officers and managers.

Finally, the Malmquist productivity index (MPI) can be introduced to measure the efficiency of firms. In the future, the well-verified MOP-based DEA model can be applied to all other performance evaluation problems and provide highly trustworthy results.

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